An industrial design approach, implementation, and application: Perspectives of surveillance radar systems [Plenary session]

Conference Paper · September 2020

DOI: 10.1109/NRSC49500.2020.9235113

CITATIONS
4

READS
487

7 authors, including:

K. F. A. Hussein
Electronics Research Institute
132 PUBLICATIONS **807** CITATIONS
SEE PROFILE

Alaa Hafez
Alexandria University
139 PUBLICATIONS **359** CITATIONS
SEE PROFILE

Fathy Ahmed
Military Technical College
76 PUBLICATIONS **203** CITATIONS
SEE PROFILE

Mohamed Mabrouk
University of Ottawa
43 PUBLICATIONS **197** CITATIONS
SEE PROFILE

An Industrial Design Approach, Implementation, and Application Perspectives for Surveillance Radar Systems

Esmat Abd-Elfattah[1], Abd-El-Rahman El-Bardawiny[2], Nabil Girgis[2], Khaled Hussein[2], Alaa S. Hafez[3], Fathy M. Ahmed[2], Mohamed Mabrouk[3], and Technical Crew

[1]Electronics Research Institute, Ministry of Scientific Research, Egypt
[2]Military Technical College, Ministry of Defence, Egypt
, Air Defense Forces, Ministry of Defence, Egypt[3]

ABSTRACT

This paper is devoted to demonstrate the most important keys to interface the design and implementation of radar systems with industrial considerations to achieve a competitive radar product. The investigation is focusing on the industrial design ideas for radar systems by formulating the advanced design concepts, system engineering design requirements and disciplinary perspective for radar production. Industrial design is synergic the industrial society, which makes originally isolated disciplines contact and interact each other to form an organic unity. It implements science, technology and creative art together. Science and technology objectively reveal the laws of nature and creative art dynamically. It doesn't only seek for unity of radar subsystems but also interested in product coordinate, human resources and environment. The implementation of the approach is demonstrated through systems engineering design rules for all radar system disciplines including, electronics, microwave, antenna, computer, digital signal processing and electrical power engineering.

Keywords: Surveillance Radar, Stripline Antenna, Digital signal processing and Data processing

I. INTRODUCTION

Radars have been used in multiple military and civilian applications. The development of the ideas that lead to the radar systems emerged in the late nineteenth and early twentieth centuries. However, the main developments of the system have been seen during the second world war. During that period radars were extensively used for air defence purposes such as long-range air surveillance and short-range detection of low altitude targets. In the post-war period, improvements had been made in the development of the radar technology for both the military and civilian applications. Major civilian applications of the radar that emerged during that period were the weather radar and the air-traffic control radar that used to ensure the safety of the air traffic in the airports [1].

Since the late 1980's, many industry organizations had moved from a hard core, technical leadership culture which depends on the art to one of systems management as a science called system engineering [2-7]. History had shown that many projects dominated by only one of these cultures suffer significant ill consequences. Organizations that focus mainly on systems management often create products that fail to meet stakeholder objectives and cost benefit analysis. To achieve mission success, must identify and develop systems engineers that are highly competent in both technical leadership and systems management. That is why we focus on the complete systems engineer, who embodies the art and science of systems engineering across all phases of radar manufacturing. The scope of systems engineering and the associated roles and responsibilities of a system engineer in any project are often negotiated by the project manager and the systems engineer [8-12]. The paper summarises how the systems engineer is dealing with the different disciplines of electrical engineering and employed them for producing the surveillance radar system with competitive price.

II. Design Procedures

A. System Engineering Concept

System engineering is the art of management of the complexity. It integrates all of the disciplines and specialist groups into a collaborative team forming a developed structure process that proceeds from concept to production and operation. Based on the design specifications, there may be variety of objectives such as those

illustrated in Fig. (1a). These requirements may be mutually supportive by nature, or there may be some inherent conflicts to achieve the goals. These goals are viewed in terms of relative importance, and design optimization is accomplished through trade off studies with the objective of establishing a mutually satisfactory approach in response to the specification and established goal. Certain categories of engineering expertise are identified as being necessary for the design and development of the system.

The system engineer received the request for quotation (RFQ) from the stakeholder which consists of three sections. The first section consists of the object, and general specification required for the product. The second section states the complete system specification required, and the third one includes technological constrains for the radar system. The design process starts from assigning the radar system block diagram, frequency band, type of the wave form, pulse duration, pulse repetition frequency, peak power, and the antenna specifications. The system is developed through the life cycle which model have evolved significantly over the past two decades. Fortunately, the life cycle model subdivides the system life into a set of basic steps that separate major decision milestones. First, the steps in the life cycle have to correspond to the progressive transitions in the principal systems engineering activities. Second, these steps have to be capable of being mapped into the principal life cycle models that is in use by the systems engineering community. The derived model will be referred to as the " systems engineering life cycle, ". This process is depicted in Fig. (1b) and contains four major activities: requirements analysis, functional analysis and allocation, synthesis, and systems analysis and control. The component tasks are presented within each activity. Although this industrial standard is no longer in use, it is still used as a guide and is the foundation for understanding the basics of today's systems engineering processes. The radar is simulated using computer aided design tool (CAD) to demonstrate the predicted beam pattern and coverage diagram at different target cross section area (RCS) as shown in Fig. (2).

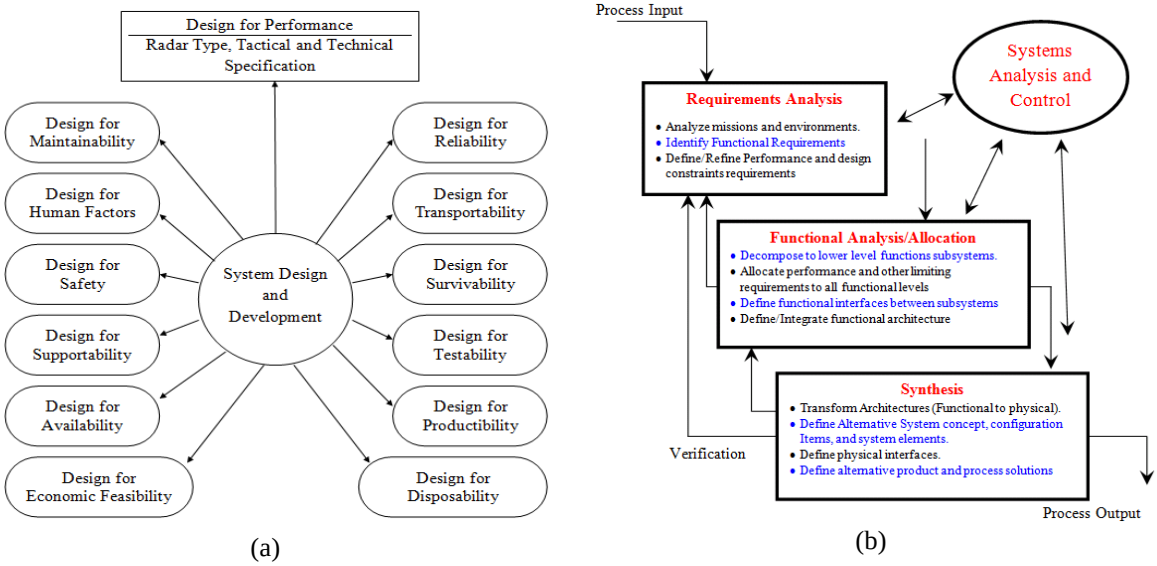
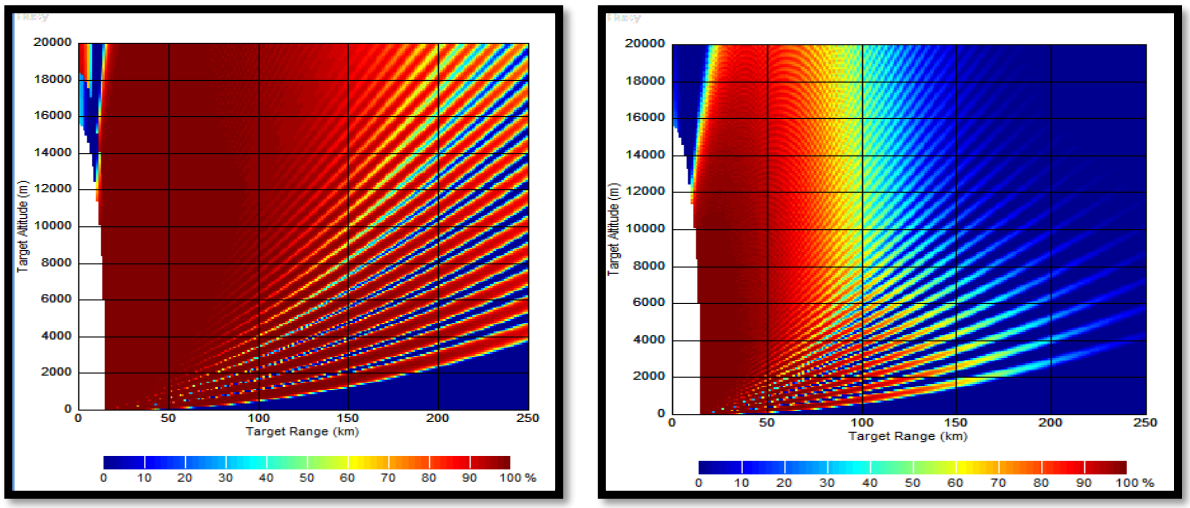


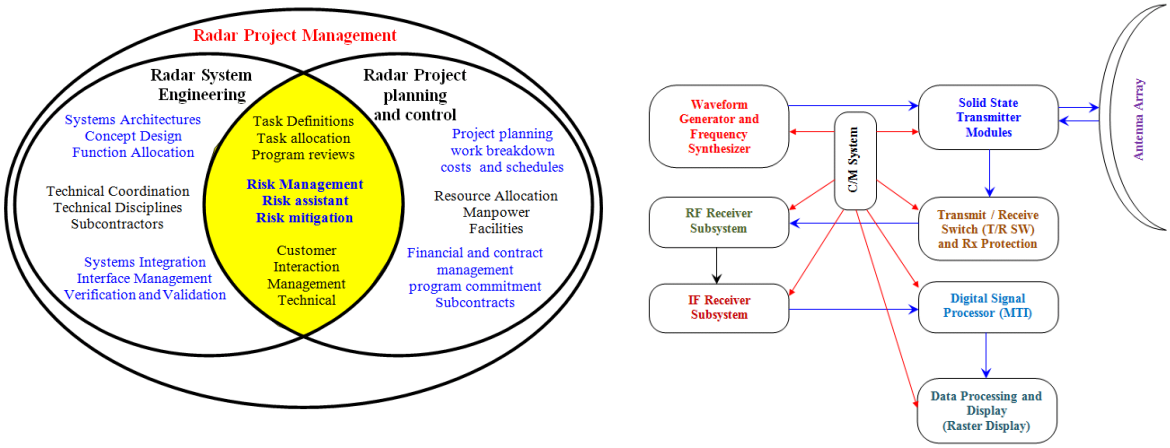
Fig. (1) : (a) System design requirements, (b) The standard system development process.

Application of the systems engineering approach evolves over the life cycle as the system progressively materializes, the focus shifts from system level during needs analysis down to component and part levels during engineering design. Testing is a process to identify the unknown design defects as it verifies the system specifications ; therefore, test planning and analysis is a prime systems engineering responsibility. Systems engineering is an essential part of the management of a system development project. The part that systems engineering plays in the project management is pictured in the Venn diagram of Fig. (3a). The ovals in the diagram represents the domain of project management and those of its principal constituents: systems engineering and project planning and control. It is seen that both constituents are wholly contained within the project management domain, where technical guidance being the province of systems engineering, while program, financial, and contract guidance are the province of project planning and control. The allocation of resources and the definition of tasks are necessarily shared functions. The complete radar block diagram is illustrated in Fig.(3b) and shows that the system is composed of eight subsystems, frequency generator, transmitter, antenna, RF receiver, IF receiver, digital signal processor, data processing, and the control and monitor system [13-23].



(a) (b)

Fig. (2) : Coverage diagram (a) RCS = 3 m^2, (b) RCS = 0.1 m^2.



(a) (b)

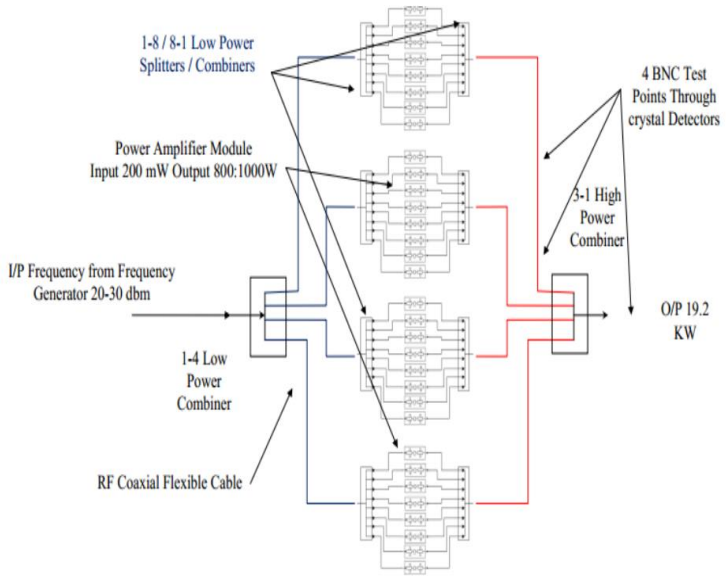
Fig. (3) (a) The relation between system engineering and project management
(b) Radar system block diagram.

The system engineer produce four documents for the disciplines designers includes, concept description sheet that describe the subsystem as a whole, inputs, outputs and control signals. The second document is the proposed subsystem block diagram from the system engineer. The third is the detailed specification of the subsystem as shown in Fig. (4) and the fourth is the design constraints. The discipline designer obligated to produce the following documents, the subsystem schematic diagram design, the simulation results of the designed subsystem, list of components used in the design aided with the detailed datasheets and vendors, apply and clarify all system engineering design rules in the design, method of test the subsystem, the requirements from low voltage power supplies, and the proposed mechanical construction required for the subsystem for the mechanical department.

B. Frequency Generator and Transmitter Subsystems

This section is to present the most important aspects of the design and implantation of frequency generator and the RF/microwave transmitter subsystems according to the required specifications. Firstly, the frequency generator design starts with establishing the critical requirements including frequencies, efficiencies, phase noise, modulations, average power and peak power. Further parameters that should be considered include linearity, DC power allocations, thermal dissipations, harmonic levels and noise power. There are different issues, but equally critical factors such as reliability, vibration, humidity, temperature, packaging, interfaces,

size, weight, and even surface textures, appearance, and colour. Safety requirement further are respected, particularly when high RF/microwave power or high voltage levels are considered. In addition, shielding against high levels of RF/microwave power and high voltages is the most important issue. The first version of the frequency generator was designed to generate RF pulsed signal which to be amplified through the transmitter subsystem as shown in Fig (5) .



No.	Function	Specification
1	Pulse Duration	100 µsec
2	Transmitted Pulses per Bursts	1
3	Duty Cycle	5 %
4	PRF	500 PPS
5	PRT	2000 µsec
6	Staggered PRF	500 PPS ±5 % 3 pitch/cycle
7	Dead Time	300 µsec
8	Maximum Range	250 Km
9	Minimum Range	15 Km
10	No. of Channels	20 with 10 MHz Separation
12	Tx Pulse Output Frequency	1200:1400 MHz
13	Input Power	10:19 dbm
14	Channel Band Width	< 1 MHz
15	Input Impedance	50 Ohm
16	Input Terminal	SMA Type
17	Control Signal Terminals	SMA Type
18	Peak Output Power	> 12 KW
19	No. of AMP Stages	Two stages (Pre-amp & amp Mod)
20	Transmitter efficiency	>30%
21	Modules i/p & o/p Impedance	50 Ohm
`22	Output Terminal	Type N Connector

Fig. (4) System engineering design documents to the disciplines.

As illustrated in Fig. (5a), the 30 MHz IF coherent signal is generated from COHO unit. COHO distribution unit is responsible for splitting and amplification of the input signal to be further sent to the IF switch and the IF receiver subsystem (IF switch is used to generate a train of pulses according to the system PRF).The signal pulse width is104µsec and the reception time is1896 µsec. The output signal is forward to the frequency mixer. On the other hand, 1200-1400 MHz RF signal is generated using frequency synthesizer and the output of the synthesizer is equally divided using equal power splitter where an output is sent to the RF receiver subsystem and the other output is filtered through the band pass filter and applied to the BPSK modulator unit. The BPSK modulator unit is used to modulate the RF signal according to the control signal generated from the FPGA kit. The modulated signal is mixed with the IF signal through the RF mixer unit. The output is further applied to the switchable filter band to be refined and sent to the transmitter subsystem. Fig. (5b) shows the second version of the frequency generator. The second version of the frequency generator was designed to enhance the performance of SNR that introduced by version (I). In this version, the modular design is improved to reduce the distortion and to improve the system reliability compared to version (I). As shown in Fig. (5b), the IF 30 MHz coherent signal is generated from the frequency synthesizer unit and delivered to distribution board. The distribution board is responsible for splitting and amplifying the input signal to be further sent to the out of phase equal power splitter, which is used to divide the input power signal and forward it to the IF switch. The IF switch is used to perform signal modulation (BPSK) using the ON/OFF feature of the RF switches. The signal pulse width is 91 µsec and the reception time 1659 µsec. The output is filtered using band pass filter and the two outputs are combined using equal power combiner. The output is provided to the frequency mixer. On the other hand, 1200-1400 MHz RF signal is generated using frequency synthesizer and the output is equally divided using equal power splitter, one output is sent to the RF receiver subsystem and the other output is mixed with the modulated IF signal using the frequency mixer. The output is then applied to the switchable filter bank (SFB) to be refined and sent to the transmitter subsystem. The (SFB) output signal is applied to the RF directional coupler to get a sample from the transmitted signal to facilitate its measurement on the frequency generator subsystem. Secondly, the transmitter subsystem, which is used to amplify the output signal from the frequency generator subsystem to be transmitted to through the antenna subsystem. Our focus is to design and implement the transmitter by deploying industrial ideas and the system engineering requirements to achieve the required output power, efficiency, gain, frequency range, nature of the load, ambient conditions, isolation, signal parameters, amplitude distortion, group delay, harmonic distortion, intermodulation distortion and reliability.

The transmitter design is based on solid-state transmitter modules that use transistors, which its internal self-redundancy, the modules operate at low DC voltage and do not require liquid cooling. The reliability of solid-state RF power amplifiers is an important factor, essentially due to the massive impact of the application on the failure modes. Therefore, we must consider the reliability early in the power amplifier (PA) design cycle. The RF transistors are usually thought to be the obstacle, but they are normally perfect sufferer from some other issues, so classified the failure modes of the power amplifier as shown in Fig (6a). In this design, power solution modules (PSM) operate in L-Band pulsed radar systems are combined with other power amplifier modules (100-Watt and 200-Watt) to provide a transmitter system with 18 KW output radiated RF power. The purchased power solution module is user friendly and requires no additional tuning or impedance matching to provide 800 Watts of pulsed RF output power at 300µsec pulse width and 10% duty cycle in the band 1200-1400 MHz. This design used two schemes to provide the transmitter subsystem Pre-amplifier schematic as shown in Fig. (6b) and Fig. (7a). While the final stage power amplifier is shown in Fig. (7b).

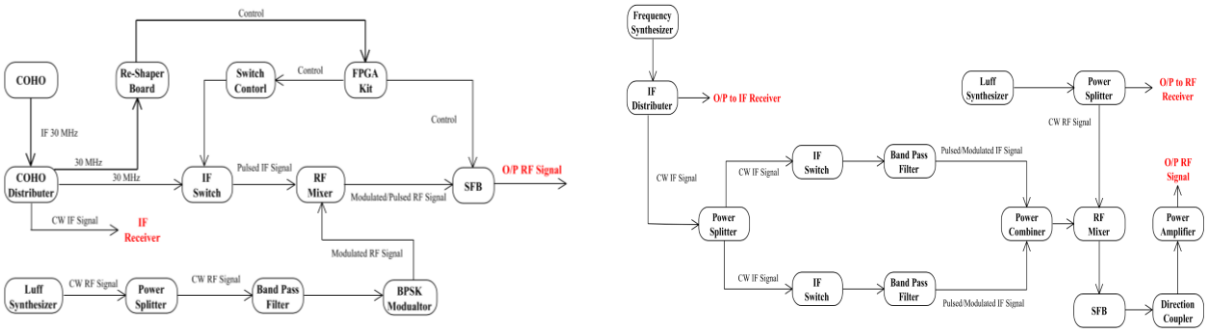


Fig. (5) : The frequency generator block diagram (a) The first Version (b) The second version.

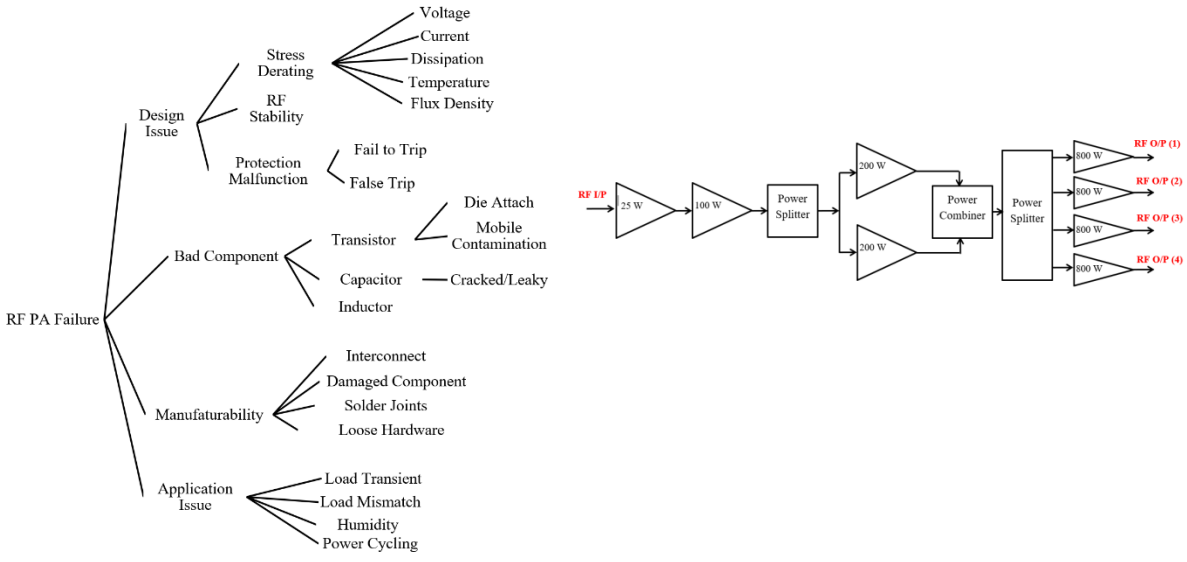


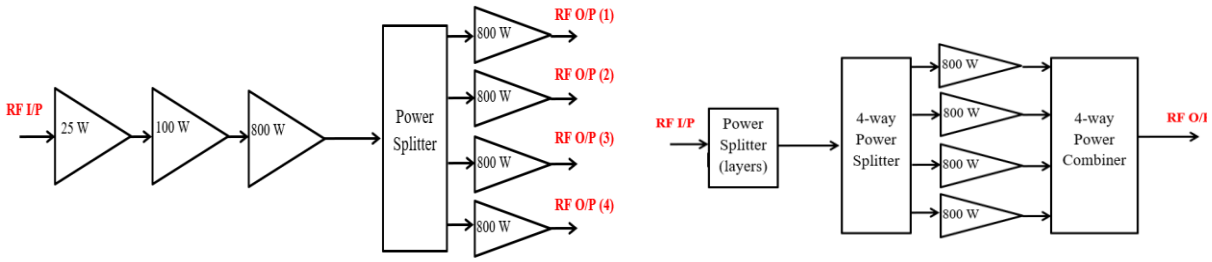
Fig. (6): (a) RF PA failure classification, (b) Schematic (A) of Pre-amplifier subsystem.

In the first version of pre-amplifier design, the frequency generator output is applied to the (25-Watt) power amplifier module as shown in Fig 4. The output is then applied to 100-Watt high power amplifier module. The output is equally divided using two-way power splitter. The output of the power splitter is applied to 200-Watt power amplifier module . The output from the two 200-Watt power amplifier modules are combined using high power RF combiner and applied to high power 4-way RF splitter . The outputs are then applied to the power

amplifier modules to be further applied to the final stage power amplifiers. According to the recognizable high losses occurred due to the excessive splitting and combination in schematic (A), a different design is introduced in schematic (B) to provide the required output power level with reduced complexity and losses. Fig 5 presents the proposed design schematic (B)for the pre-amplifier subsystem.

In this version of pre-amplifier design, the frequency generator output is applied to the (25-Watt) power amplifier module as shown in Fig. (7a). The output is then applied to 100-Watt high power amplifier module. The output is amplified again through the power amplifier module. The output from high power amplifier module is divided using high power 4-way RF splitter and forward each output to a high power amplifier module to be further applied to the final stage power amplifiers. According to our records, schematic (B) provided four stable output RF signals of amplitude higher than 59 dBm (800-Watts) using the given input from the frequency generator subsystem. Next section presents the final stage power amplification subsystems.

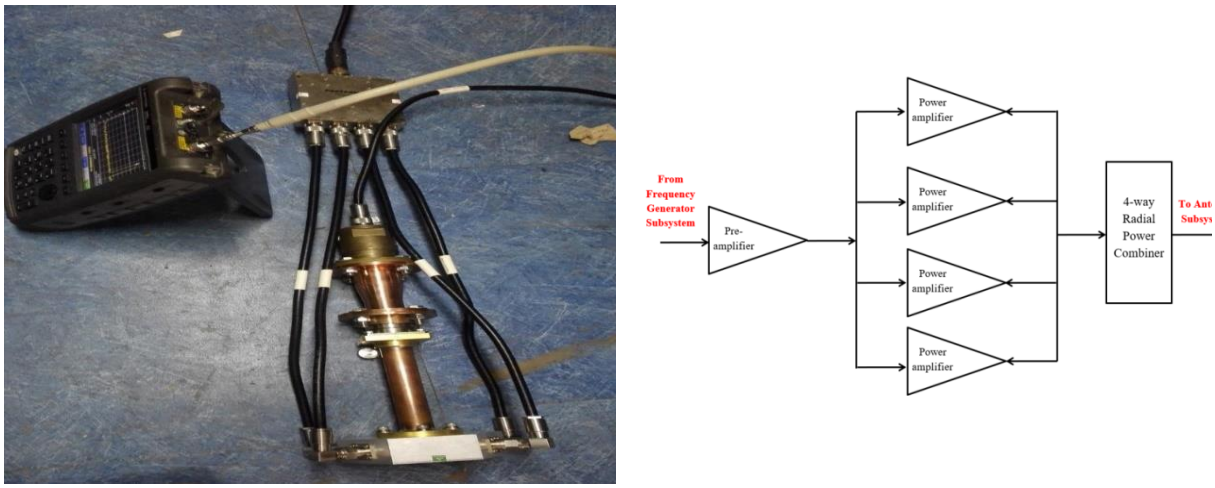
Fig. (7b) shows the schematic diagram used in the design of the final stage power amplifier subsystem. This design can be explained as follows: the RF output (800-Watt) from the pre-amplifier subsystem is forward to the 2-way power splitter in the power amplifier subsystem. The 2-way power splitter is used to divide the input RF signal equally to the top and bottom layers of the final stage power amplifier module. Each output is again applied to 4-way power splitter on each layer. Each output will be amplified using the power amplifier module separately. Then they combined using high power 4-way combiner. Therefore, it is recorded that each layer in the final stage amplification subsystem can provide 65 dBm (about 3.2 KW) RF pulsed high power signal. A final combination is done using high power 2-way power combiner to provide minimum output of 68 dBm (6 KW) minimum for each final stage power amplifier subsystem. The combination of the final stage power amplifier subsystems (4 x 6 KW) is done using high power radial combiner. That could handle up to 24 KW pulsed RF signal as shown in Fig. (7b). Moreover, we design and implement the adaptor (13-30 to 1-5/8) connected to the high power radial combiner to support the matching between the combiner and the circulator input. Fig. (8a) demonstrates the implemented adapter, while Fig. (8b) shows the overall block diagram of the transmitter subsystem using both pre-amplifier and final stage amplifiers.



(a) (b)

Fig. (7) : (a) Schematic (B) of Pre-amplifier subsystem,

(b) Schematic of the final stage power amplifier subsystem (single layer).



(a) (b)

Fig. (8) : (a) The implemented adapter, (b) Transmitter sub-system block diagram.

C. Antenna Subsystem

The main objective of this section is to design, synthesize, fabricate, measure and make field-testing for the two dimensional (2D) radar antenna array system as shown in Fig. (9) according to the stated specifications. Firstly, a new synthesis algorithm for shaped radiation patterns using linear antenna arrays with reduced number of antenna elements is introduced. The algorithm is based on a combination between two different algorithms the method of moments and the genetic algorithm (MoM/GA). It provides a robust synthesis tool for both pencil beam and shaped power patterns. The MoM is used to estimate the excitation coefficients, while the GA is used to estimate the optimum element spacing.

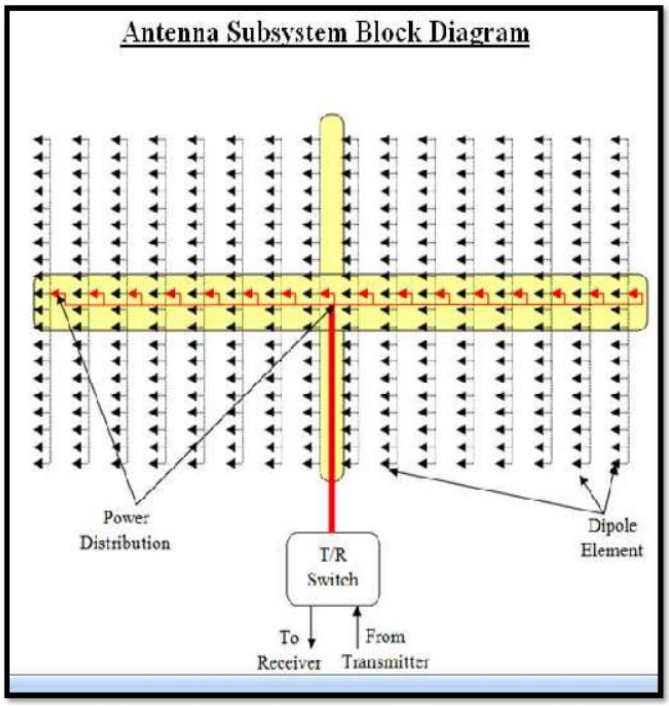


Fig. (9): Antenna system block diagram.

Unequal Wilkinson power divider is introduced as a basic element to build both vertical and horizontal feeding systems. The Wilkinson power divider is chosen as a basic element because it provides isolation between the output ports, it is capable of being matched at all ports and it becomes lossless when the output ports are matched. Compute simulation technology software (CST) simulator is used as a synthesizing tool to check the accuracy of the designed structure. The results of the simulated structure agree well with the synthesized one. Many shapes of antennas are investigated to meet the main requirements of the antenna array system. The restriction of wide bandwidth, high gain, and power handling capability on lower and upper frequencies are mutually conflicting and hence a design compromise is adopted. The need for portability implies the use of electrically small antennas, which consequently results in a low gain and associated broad radiation patterns. The types of antennas that can be used are therefore limited. Some proposed antennas such as a bowtie-shaped strip-line antenna, folded dipole antenna, printed monopole antenna and slot antenna are introduced and investigated to meet the antenna array requirements. The folded dipole antenna is selecteed, which achieved the required bandwidth, gain, support high power in addition to a smaller size as shown in Fig. (10). Then, a complete antenna array system is simulated using CST simulator and the obtained results are compared with the synthesized one. The synthesis of the radar antenna array is divided among five parts namely, vertical excitation coefficients synthesis, horizontal excitation coefficients synthesis, array element synthesis and design, vertical feeding network synthesis and design, and horizontal network synthesis and design. The simulated results using CST simulator are compared with the synthesized one and it achieves good agreements. The antenna array fabrication, measurements, and field tests are introduced and illustrated in four consequent steps, in the first step, a single column of antenna consisting of 22 radiators. It was fabricated from EN AW-6060 alloy based on strip-line technology. Return loss measurement was done using Agilent technologies N9118A vector network analyzer. The far-field measurement was carried out using an outdoor measurement system in Benha factory as shown in Fig. (11).

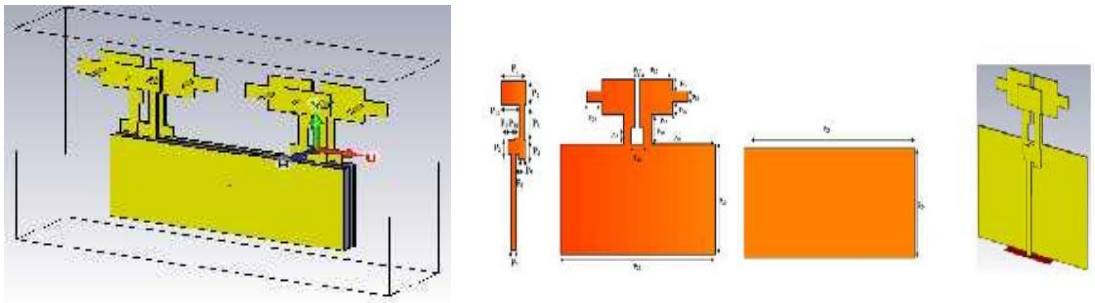


Fig. (10): Folded dipole antenna.

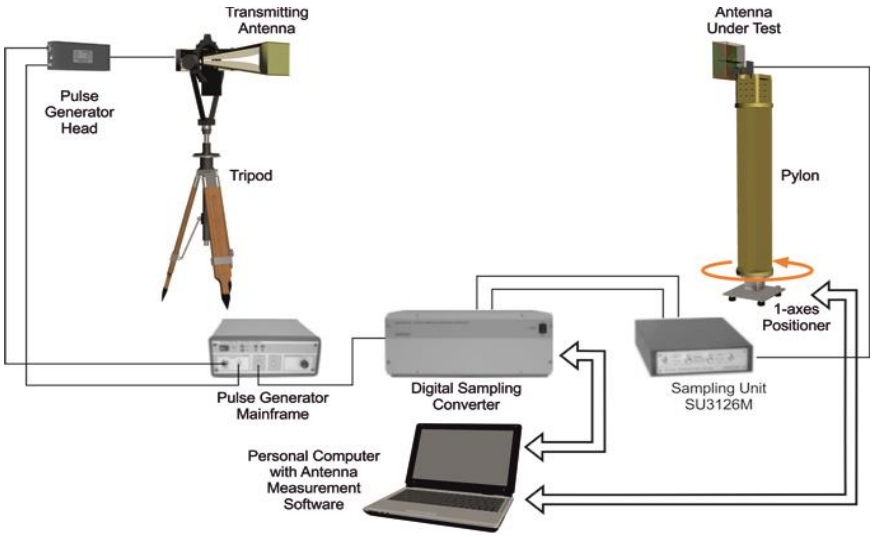


Fig. (11): Far field measurement setup of the antenna array system.

The single column operates well at the operating bandwidth. Then in the second step the return losss and far field are measured for two columns and the return loss result is below -10 dB at the operating bandwidth. Furthermore, the measurement of the elevation radiation pattern shows that a 3 dB beamwidth of 360 is obtained.

In the third step, three identical columns are assembled and measured to investigate the effect of coupling on the proposed antenna array. The measured results are found to be very promising. Teflon material with 1 mm thickness and $\in_r$= 2.1 is used to build radome of the columns as shown in Fig. (12a). Radome has proven to be very effective when considering life cycle cost, since the antenna is contained in a protected environment, maintenance cost are held to be minimum. The 3 dB elevation beamwidth for one column is changed by 1˚ only (from 36˚ to 37˚). The single column antenna array operates well and is not affected much by the presence of the radome. After fixing the radome material, painting of both outer surfaces of the two ground sheets and the radome was done as shown in Fig. (12b). It is found that painting doesn't affect the 3 dB elevation beamwidth but directivity varies by 1 dBi at elevated angle 6˚ and 354˚, respectively.

(a) (b)

Fig.(12): (a) The radome installation process, (b) The painting process.

The horizontal feeding network of 32 unequal power divider was designed and analyzed. The two ground planes and the feeding network are drilled using a CNC machine. The N-type connectors and the 100-ohm resistors are soldered. The nails are used to assemble the whole horizontal feeding network as shown in Fig. (13). The horizontal feed S-parameter ensures that the required operating bandwidth is achieved. The fourth and the last step is the overall antenna array measurements. The 32 identical columns are assembled. Each column contains internal strip-line circuitry that acts as an RF power splitter to distribute the RF energy to the 22 vertically polarized dipole elements. The outdoor measuring setup is used to measure the radiation pattern at four different frequencies 1.2 GHz, 1.3 GHz, 1.35 GHz, and 1.4 GHz as shown in Fig 9. Different parameters are measured namely return loss, elevation and azimuth 3 dB beamwidth, gain, side lobe level, etc.

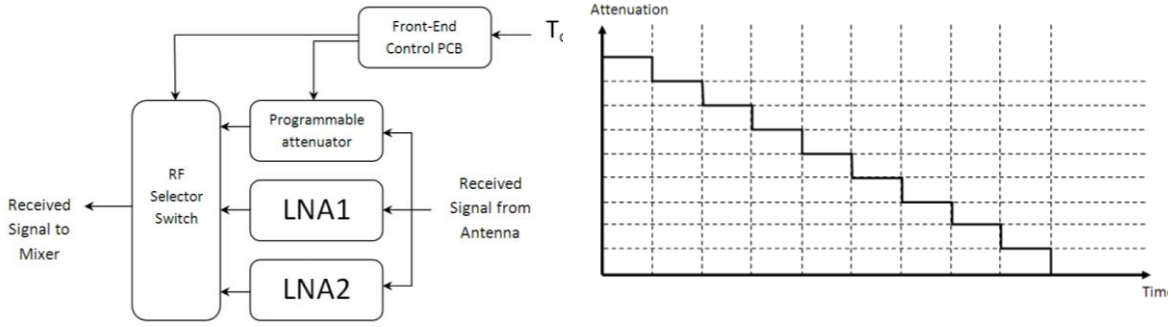
Fig. (13): The assembly process and radiation pattern outdoor measuring setup.

D. RF Receiver Subsystem

The main function of the radar front-end is to protect the radar receiver from large power echoes returned from near targets and amplify the low power echoes returned from far targets. It has gain control waveform begins with pre selected high attenuation at the origin of the sweep and reduces the attenuation as the range increases. This section describes a dynamic RF front-end implemented for radars. This system increases the probability of detection (PD) of the radar for medium and far range targets. The implemented system is based

on dividing the receiving time into two sections; the first section includes the echoes returned from near targets with relatively strong power. The second section includes the echoes returned from medium and far targets with relatively low power. The sensitivity time control (STC) system is adopted in the first section to protect the radar system from saturation and increase the dynamic range. The second section is divided into two regions; the first region uses a high gain with relatively medium noise figure low noise amplifier (LNA) and second section uses a medium gain with low noise figure LNA. The implemented system is designed and simulated under Matlab program environment and the CAD tools. The second section is divided into two regions switched dynamically between two LNA's. The first LNA is a two stage LNA with 33 dB average gain and 1.9 dB average NF. The second LNA is a one stage LNA with 17 dB average gain and 0.45 dB average NF. The two LNA's are switched between these two regions to achieve a maximum amplification with the medium range targets and minimum noise figure with far range echoes which may be confused by the noise.

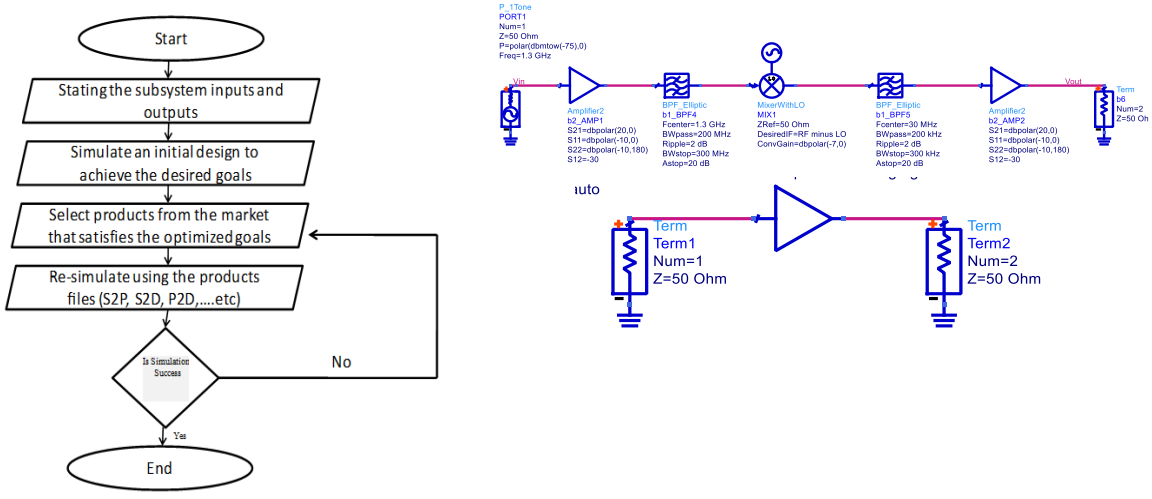
The block diagram of the implemented system is shown in Fig. (14a). The received signal is passed to the three main components programmable attenuator, LNA1, and LNA2. The front-end control printed circuit board PCB receives transmit zero signal from synchronizer PCB and controls the operation of RF selector switch. The STC waveform is shown in Fig. (14b). STC is used to control the gain of the radar receiver. The surveillance radar detects echoes from widely differing amplitudes, typically so great that the dynamic range of any fixed gain receiver will be exceeded. The effect of range on radar echo strength overshadows the other causes; however, the echo power received from a reflective object varies inversely with the fourth power of the range or propagation time of the radar time.



(a) (b)

Fig. (14) : (a) The Implemented dynamic front-end system, (b) STC waveform.

System simulation is carried out using Advanced Design System ADS2013 from Agilent. ADS CAD tool features simulation and analysis of the overall system using RF Budget simulation and measurement facility. The design flow will be described in the flowchart shown in Fig. (15a). Fig. (15b) shows the cascaded components used in the design of RF receiver subsystem. According to the previous flow chart, subsystem input and output should be clear and well defined. Component simulations are done individually using the product measurement files (S2P, S2D, P2D…) to verify that each component satisfies the required goal.



(a) (b)

Fig. (15) : (a) Flow chart presenting design and simulation process
(b) The cascaded components used in the design of RF receiver subsystem.

E. IF receiver

The objective of the intermediate frequency receiver (IF-Rx) is to detect, amplify, filter and down convert the radio frequency (RF) signal to baseband video signal that can be delivered to digital signal processing (DSP) sub- system. Fig. (16) shows the general block diagram of an analog IF receiver. The IF-Rx consists of two main parts: The Dickie fix circuit and the analog down converter. The Dickie fix circuit consists of amplifier, narrow band pass filter and limiter. The analog down converter part consists of I and Q double balanced mixer, low pass filter, video amplifier and analog to digital converter (ADC) chips. ADC chips can be mounted on the IF receiver card or at the front of the DSP electronic card. However, designers prefer to mount them on the DSP card to apply testability requirements easily.

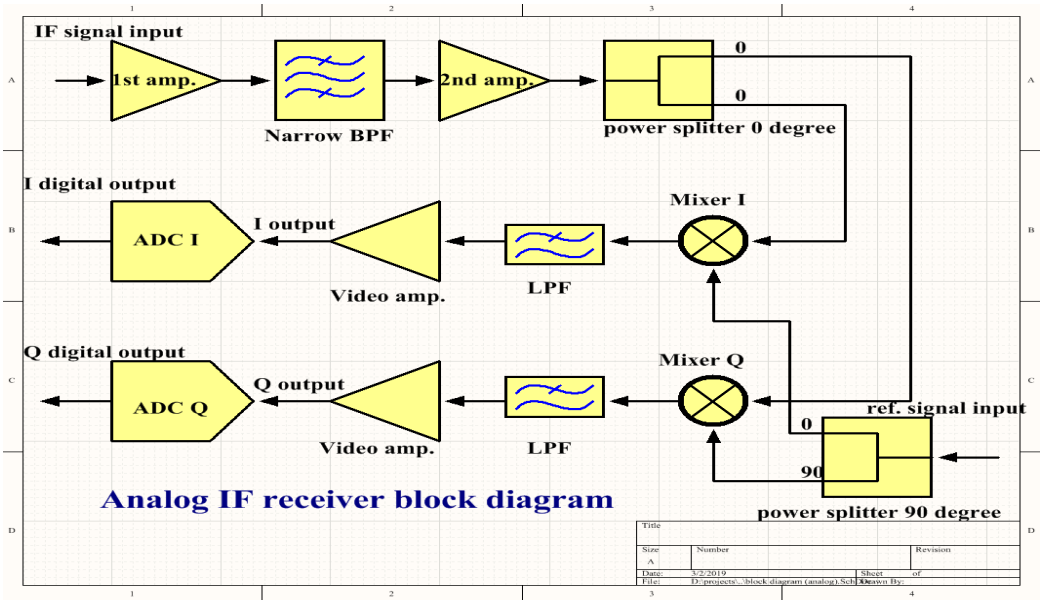


Fig. (16): Analog IF receiver general block diagram.

The main parameters that describe the performance of the IF-Rx are sensitivity, dynamic range and chain noise figure. Sensitivity of the IF-Rx is the minimum detectable signal level at a certain output signal-to-noise ratio(SNR) according to system requirements. It can be measured by injecting a signal with minimum acceptable SNR and different power levels. Then, record the minimum detectable signal at the IF-Rx end. The dynamic range is the difference between the minimum detectable signal and the maximum acceptable signal. It can be calculated by injecting a signal and measure the output then increase the input power level until receiver saturates. The difference between that level and the minimum detectable signal that has been measured form sensitivity test is the dynamic range. The chain noise figure is the ratio between input SNR and output SNR.

There are many other parameters that can affect the performance of the IF-Rx. These parameters are system internal noise level, electromagnetic interference (EMI) and electromagnetic compatibility (EMC). System internal noise level can be reduced by enhancing printed circuit board (PCB) layout, thermal analyses and good decoupling. EMI can be reduced by isolating the circuit from other circuits using ferrite beads at the power traces. In addition to, shielding sensitive signal traces and good shielding enclosure for the PCB. The shielding enclosure protect the If-Rx from the electromagnetic waves radiated by other boards and the leakage from transmitter to get better EMC.

For IF-Rx testability the test points for each node are added. For maintainability each through hole integrated circuit (IC) is placed on base for easier replacement. Also, the silk screen of the board shows notes for the board powering pins and the gain control limits. The technical design documents include test procedure, bill of materials and assembly drawings of the PCB should be available. A test bench is designed for testing every node of the board to achieve the highest test accuracy.

F. Digital IF Receiver and Digital Signal Processing

Analog IF receiver is implemented as shown in the radar system block diagram of Fig. (3b). The output IF signal from the RF receiver is amplified using a wide band amplifier. Then it is passed through a Dicefix circuit to limit the jamming effect. The main part of the analog IF receiver is the analog phase detector, where the received IF signal is mixed with the reference IF signal to produce the in-phase and quadrature base band signals, I & Q. This process is called quadrature demodulation. These base band signals are then converted into digital form to be processed by the digital signal processor.

Recently, digital IF receivers are introduced in modern radar systems to reduce the high-cost, large-size, and inflexibility problems of traditional versions [24]. In this section, a proposed digital IF receiver as well as an advanced digital radar signal processor with a digital waveform generator are introduced. The design principle, simulation, and hardware implementation issues based on Field Programmable Gate Array (FPGA) for the proposed architecture are discussed.

Fig. (17) shows the general block diagram of the proposed digital IF receiver and DSP. The proposed design is introduced for two cases; the first case is Barker 13 phase coded signal, and the second one is compound 169 Barker phase coded signal.

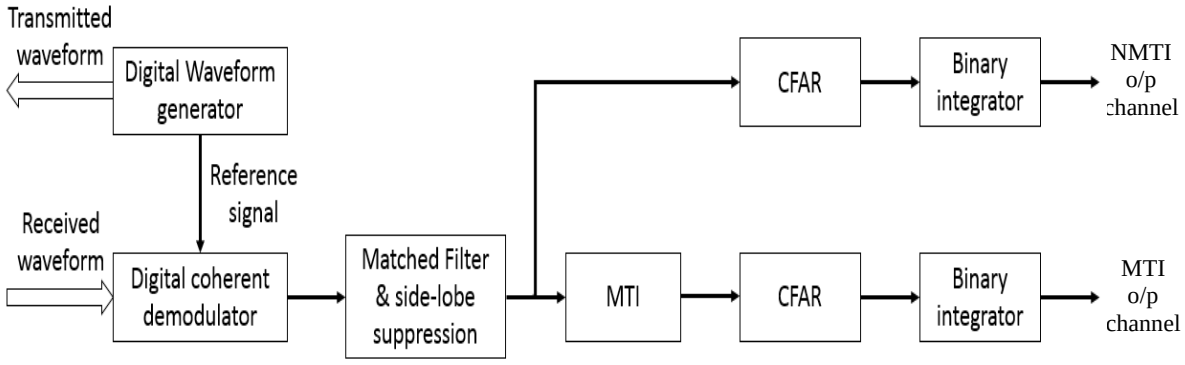


Fig. (17) The block diagram of the proposed digital IF receiver and DSP.

F.1 Digital Waveform Generator

Radar waveforms used to be generated using analog devices in old radar systems. The analog waveform design imports constraints on the generated waveform. In modern radar systems, radar waveform can be generated using real-time direct digital synthesis of analog waveforms, which can be implemented using FPGA's and digital to analog converters. In the proposed processor, a digital radar waveform generator is introduced. This waveform generator can be used to generate different waveforms. In the present work, it is used to generate two different waveforms; The first waveform is a pulse with a pulse width of 104 µs modulated with Barker-13 code. The second generated waveform is a pulse signal with a pulse width of 100 µs and a PRT of 2000 µs, coded with compound Barker-169. Fig. (18) shows the block diagram of the proposed waveform generator. The modulated pulse is generated by selection between sine and cosine waveforms according to the required Barker code.

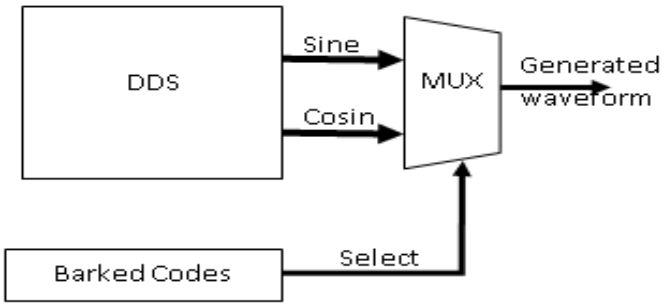


Fig. (18) Waveform generator block diagram.

F.2 Digital Coherent Demodulator

The coherent demodulator, also called a Phase-Amplitude Demodulator (PAD), working at a sampling frequency of 245.76 MHz, this is followed by down-sampling to achieve 125 KHZ for Barker 13 and 1.7 MHz for compound Barker 169. The coherent demodulator demodulates the IF signal to provide two orthogonal signal vector components, sinθ and cosθ [25].It consists of a digital multiplier that multiplies the received signal with reference 30MHz sine component for the in-phase (I) channel and 30MHz cosine component for the quadrature-phase (Q) channel. After multiplication, a low-pass filter is applied to remove the undesired high-frequency components and to keep the envelope only. The low-pass filter is designed using window method. A Hamming window is used with 21 coefficients resulting in 47dB stop-band attenuation [26]. Both I- and Q-signals for Barker 13 and compound Barker 196 are shown in Figs. (19) and (20) respectively before low-pass filtering and after applying the designed low-pass filter. It is noticed that the high-frequency component is completely removed and the Barker code is left.

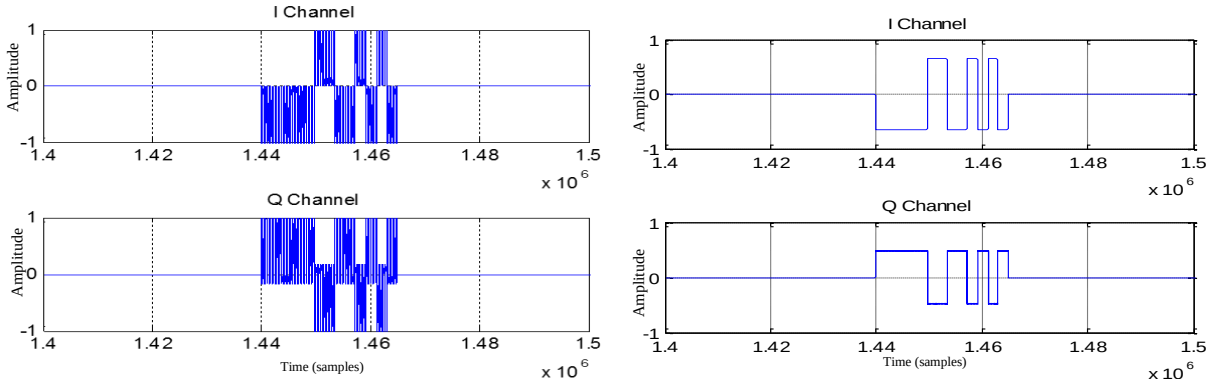


Fig. (19) Barker 13 I/Q signals (a) before low-pass filter and (b) after low-pass filter.

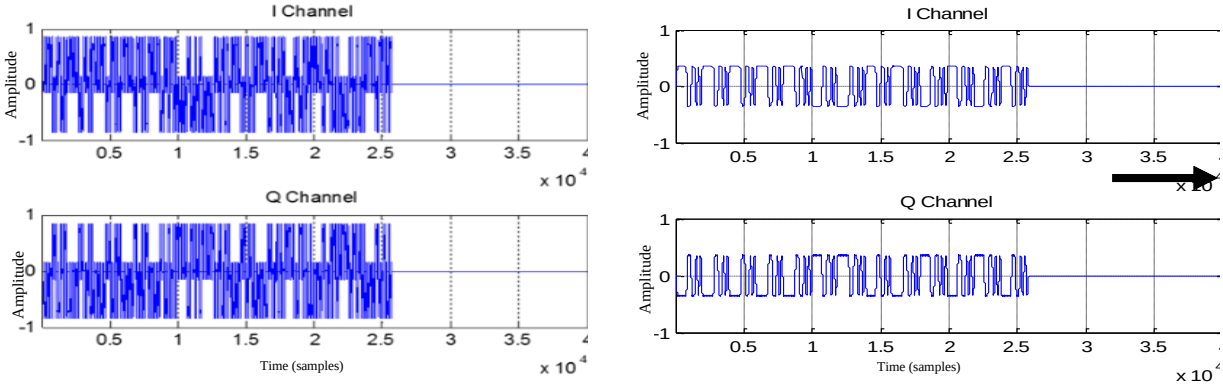


Fig. (20): Compound Barker code I/Q signals (a) before low-pass filter and (b) after low-pass filter.

F.3 Matched Filter Design

The matched filter is a filter whose impulse response is a replica of the transmitted signal. The matched filter can be designed using two methods: either the direct convolution method (time domain) or the fast convolution method (frequency domain).The choice between both methods is done according to the length of the impulse response. The direct convolution method means direct filtering that the time domain replica samples of the transmitted signal are used as coefficients in a Finite Impulse Response (FIR) filter convolution in time domain is equivalent to multiplication in frequency domain and vice versa. When using long impulse responses (filter kernels), multiplication in frequency domain is the more efficient of the two methods [27]. Implementation of the matched filter in frequency domain is shown in Fig. (21).The simulation results for the matched filter output for both Barker 13 and compound Barker 169 are shown in Fig. (22).

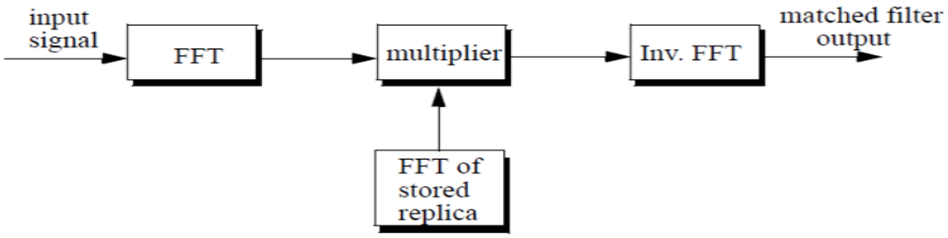
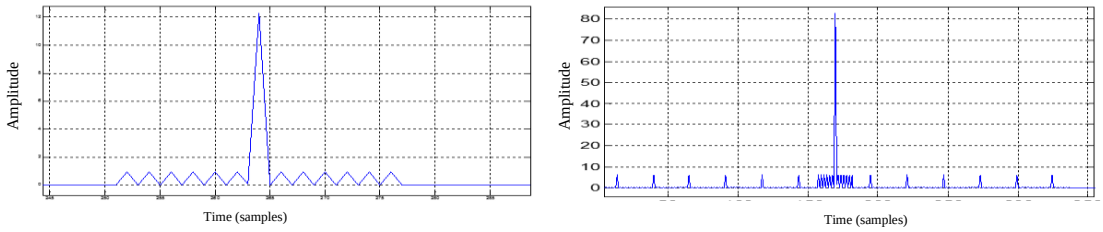


Fig. (21) Matched filter using fast convolution.

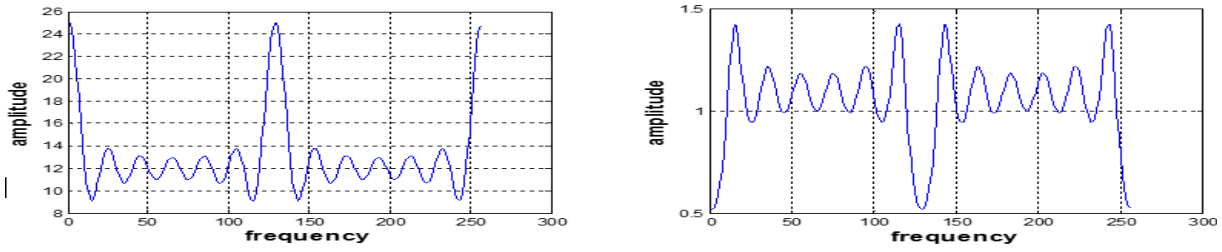


(a) (b)

Fig. (22)Matched filter output for (a) Barker 13 and (b) compound Barker 169.

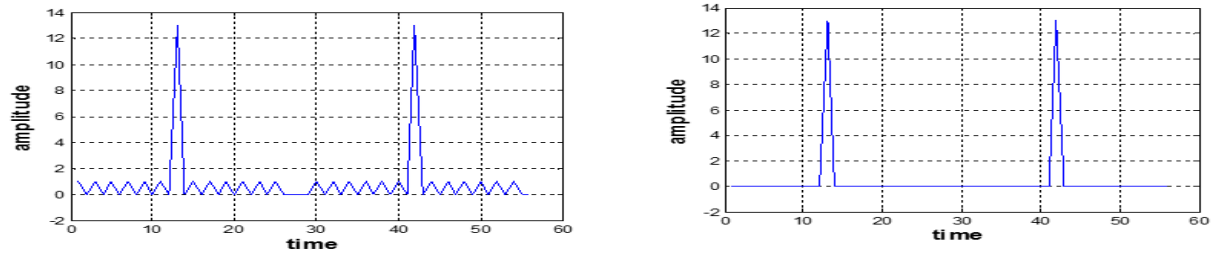
F.4 Side-Lobe Suppression

The optimum filter proposed in [27] which is used for time range side lobes suppression is a filter whose impulse response is equal to the spectrum of the correlation function of the transmitted signal without time-side divided by the spectrum of the correlation function of the transmitted signal. The advantage of the optimum filter over other side-lobe reduction methods is that it does not reduce the amplitude of the time-side lobes; but it completely suppresses it. Another advantage over the mismatch filter is that it does not affect the amplitude of the input signal. Therefore, there is no bit growth in the word length at the filter output and no extra hardware resources are required after the optimum filter due to bit growth. Both the frequency domain of the output of the matched filter and the frequency response for Barker 13 optimum filter are shown in Fig. (23). The result of the optimum filter is shown in Fig. (24). The optimum filter increases the main-to-side lobe ratio for Barker 13 from 22.3 dB to 369.1658 dB. For compound Barker, both the frequency responses of the matched and the compound Barker code optimum filter are shown in Fig. (25). The output of the two filters is shown in Fig. (26).



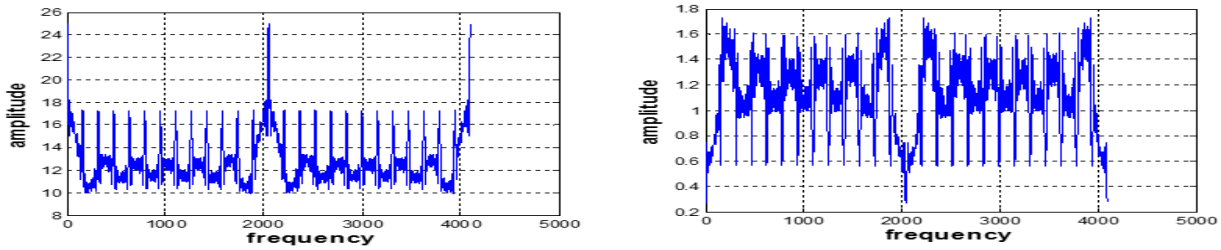
(a) (b)

Fig. (23), (a) Frequency domain of Barker 13 correlation function and (b) Frequency response of Barker 13 optimum filter.



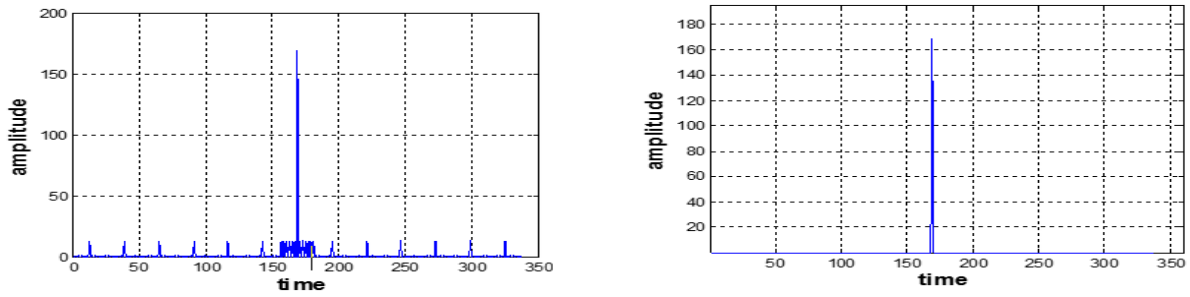
(a) (b)

Fig. (24)Barker 13 correlation function (a) before optimum filter and (b) after optimum filter.



(a) (b)

Fig. (25)(a) Frequency domain of compound Barker correlation function and (b) Frequency response of compound Barker optimum filter.

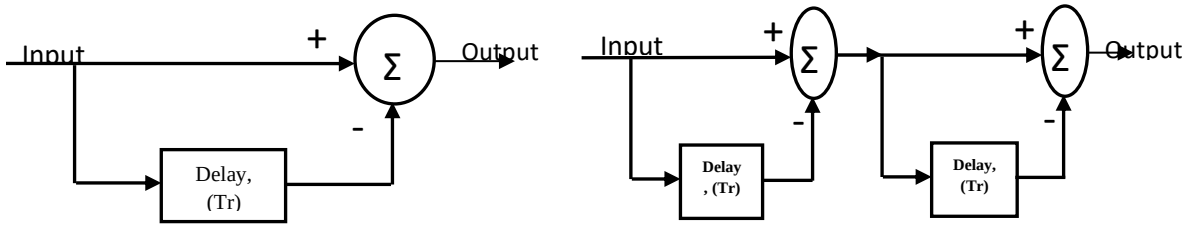


(a) (b)

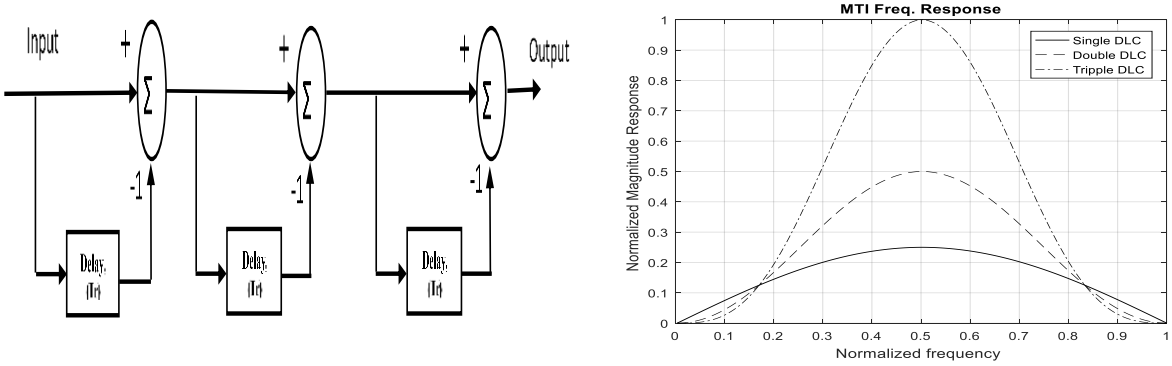
Fig. (26) Compound Barker correlation function (a) before optimum filter and (b) after optimum filter.

F.5 Moving Target Indicator (MTI)

The purpose of an MTI filter is to suppress target-like returns produced by clutter, and allow returns from moving targets to pass through with little or no degradation [29]. MTI may be implemented as single, double, or triple Delay Line Canceller (DLC) as shown in Fig. (27a), (27b), (27c). The normalized frequency responses of these MTI structures are shown in Fig. (27d).Single delay line canceller are favorable in LFMCW radars to detect slowly moving targets like walking persons. On the other hand, double or triple delay line cancellers are more favorable than single delay line canceller in air defense radars because they have a wider notch at the stop band to reduce the effect of slowly moving unwanted signals like chaffs. The used MTI structure in the proposed work is the double delay line canceller.



(a) (b)



(c) (d)

Fig. (27) Realization and frequency response of MTI

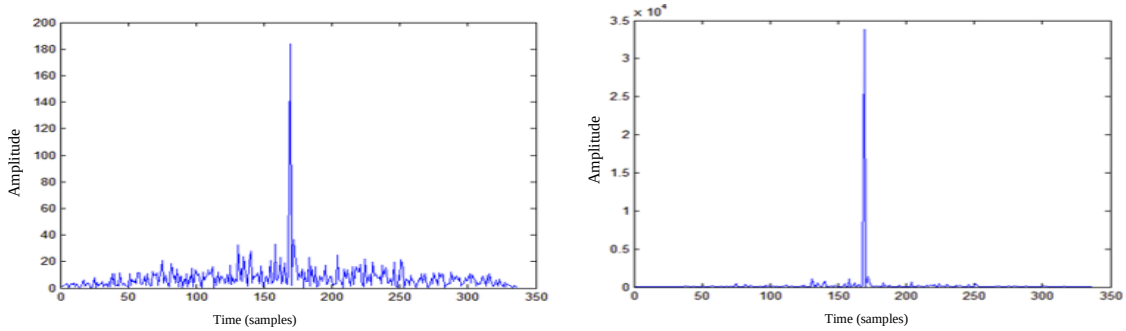
(a) Single DLC, (b) Double DLC, (c) Triple DLC, (d) MTI Frequency Responses.

F.6 Magnitude Calculation

The magnitude of both the I- and Q-signals must be calculated before sending the output of the MTI or matched filter to the CFAR detection. The magnitude calculation is done by summating the square of the I-signal and the square of the Q-signal, then calculating the square root of this sum. Fig. (28) shows the effect of calculating the square root or not of the signal before applying it to the CFAR detection for SNR at the receiver input of 0 dB. The result shows clearly that the ratio between the amplitude of the echo signal and the amplitude of the noise is increased when dealing with the square of the magnitude. In order to further study the effect of calculating the square of the signal before CFAR detection, the Receiver Operation Characteristic (ROC) curve was derived at a probability of false alarm 10^{-6} for the following cases:

- Calculating the magnitude before CFAR detection.
- Calculating the square of the magnitude before CFAR detection.
- Calculating the 4th power of the magnitude before CFAR detection.

In Fig. (29), the ROC curve shows that taking the square of the magnitude improves the probability of detection; meanwhile, taking the 4th power of the magnitude gives nearly the same probability of detection obtained by using the square of the magnitude.



(a) (b)

Fig. (28) Calculating the square of absolute signal:(a) Signal before square and (b) Signal after square signal.

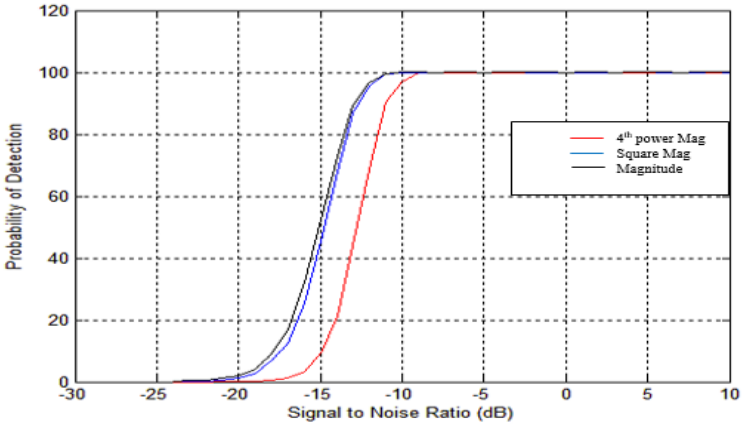


Fig. (29) ROC curve at the output of the CFAR.

F.7 Constant False Alarm Rate (CFAR)

After the magnitude calculation for the output of both I and Q channels of the MTI, this magnitude value is fed to CFAR to take the decision. The implemented CFAR is the Greatest-of CFAR (GOCFAR) with 27 cells. The simplified block diagram of the implemented GOCFAR processor is shown in Fig. (30a). Two guard cells around the test cell are introduced such that the summation of leading and lagging windows are not affected by

the target returns in the test cell. The value of the required false alarm probability depends on the value of the multiplication factor (threshold factor), which is less than one. Fig. (30b) shows the threshold and decision of the CFAR for an echo signal of a moving target with $f_{Doppler} = 0.5\ F_r$ and with SNR of 0 dB at the receiver input, where Fr is the pulse repetition frequency.

The used binary integrator in this design is an adaptive binary integrator based on CFAR output. The output of the CFAR is applied to a delay line chain. Each delay element possesses a delay time equal to the radar pulse repetition period (Tr) and the number of the required delay elements is equal to the Coherent Processing Interval (CPI) length. The output of all delay lines are summed together in an adder tree. Then, the sum is compared with a threshold; if the sum exceeds this threshold, it is declared as a target. The block diagram of the binary integrator is shown in Fig. (31). The decision taken when two targets are present at SNR= 0dbm is shown in Fig. (32).

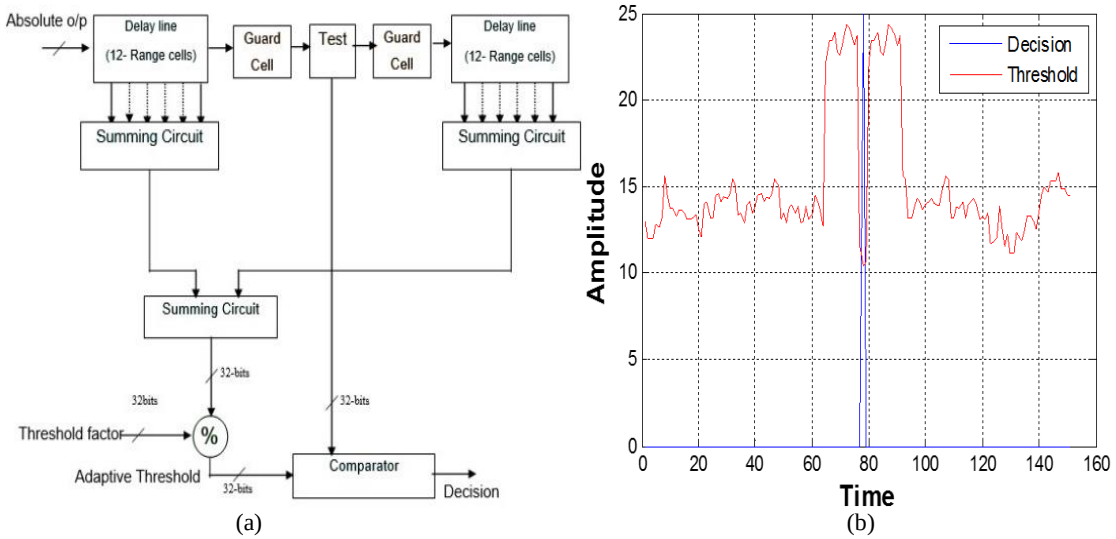


Fig. (30) Block diagram and the calculated threshold using a 27-cells GOCFAR.

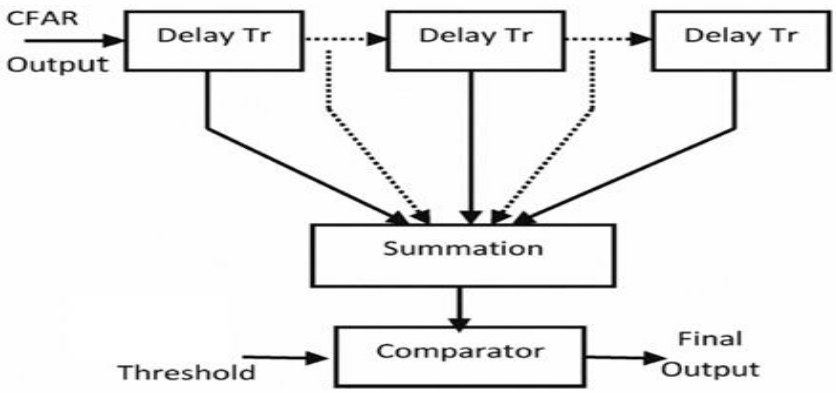
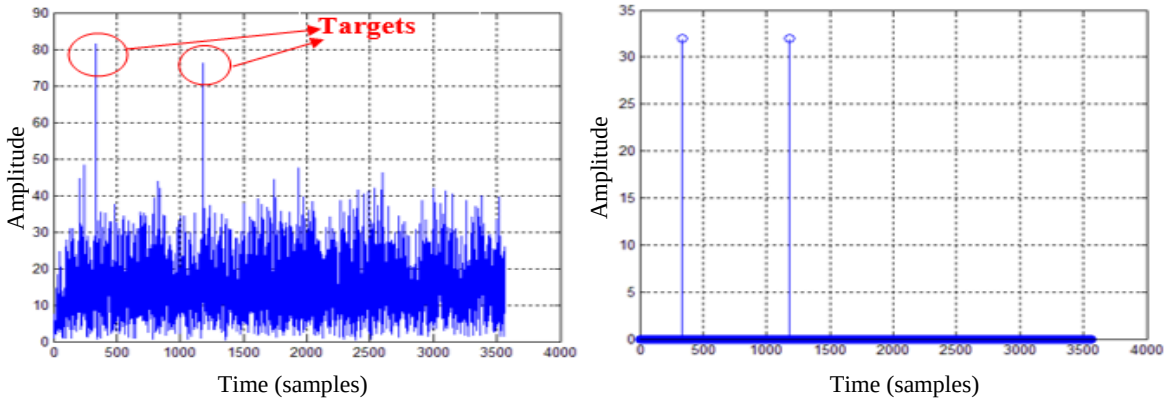


Fig. (31) Block diagram of the binary integrator.



(a) (b)

Fig. (32)(a) The output of the MTI shows 2 targets contaminated with noise and (b) The output of the binary integrator shows the detection of the two moving targets.

F.8 Hardware Implementation

The hardware implementation of the proposed work is divided into two parts, the first part of the hardware design is generating the IF binary phase coded pulse, this pulse will be used for transmission and for testing with the ability of changing the phase of the generated analog signal to simulate a returning echo from moving target. The second part of the design is the digital IF receiver and DSP which is capable of performing digital coherent demodulation, matched filtering, side-lobe cancellation, MTI filtering, CFAR detection and binary integration. The processor is designed for both Barker-13 modulated waveform and compound Barker-169. Arithmetic operations performed in the signal processor are done in single precision floating point data representation which is the same data representation used in the MATLAB design in order to have the hardware working with the same precision of the MATLAB simulations and to avoid quantization noise.

The hardware used for implementing the design is the Xilinx ML605 DSP kit, this kit includes a development board with the Virtex-6 XC6VLX240T FPGA chip which has 241,152 logic cell equivalents, 768 DSP slices and about 216 Kbit RAM which makes it a suitable FPGA for implementing complex DSP algorithms, the FPGA board is equipped with an FMC daughter board that contains TI's ADS62P49/ADS4249 dual-channel 14-bit 250Msps ADC and TI'sDAC3283 dual channel 16-bit 800Msps DAC on a daughter board. However, a photo for the used hardware is shown in Fig. (33).

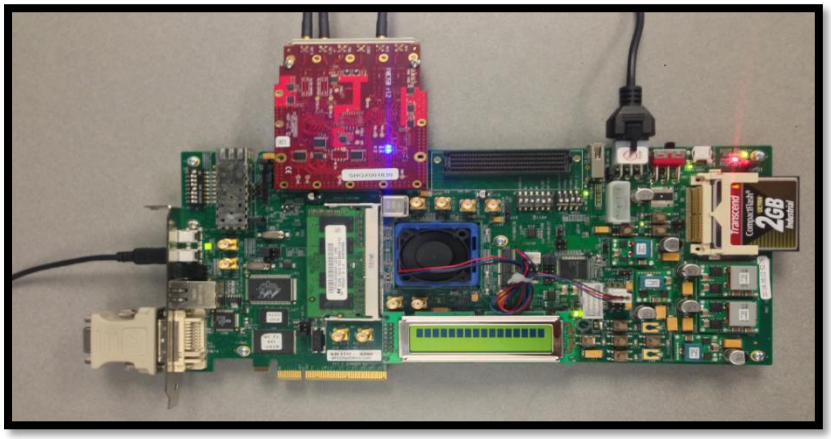
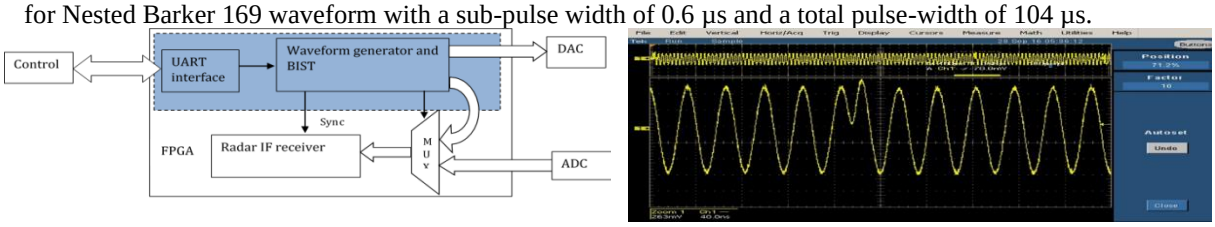


Fig. (33) A photo for the used FPGA hardware.

F.9 Waveform Generator

The waveform generator is implemented in FPGA based on [29] to generate any binary phase coded waveform for radar transmission in addition to generating an echo like signal. The echo testing signal is

generated with a predefined amplitude, predefined Doppler shift and at a specific range cell. The waveform generator is also responsible for generating the radar sync pulse. The proposed digital circuit for generating the waveform generator consists of Direct Digital synthesizer, multiplexer, phase shifting circuit, comparator and binary counter. Fig. (34a) shows the block diagram of the complete system using the radar receiver and the waveform generator. The 16-bit output of the waveform generator is connected to the DAC3283 dual channel 16-bit 800Msps DAC available in the DSP150 data acquisition card. Fig. (34b) shows the results on oscilloscope for Nested Barker 169 waveform with a sub-pulse width of 0.6 µs and a total pulse-width of 104 µs.

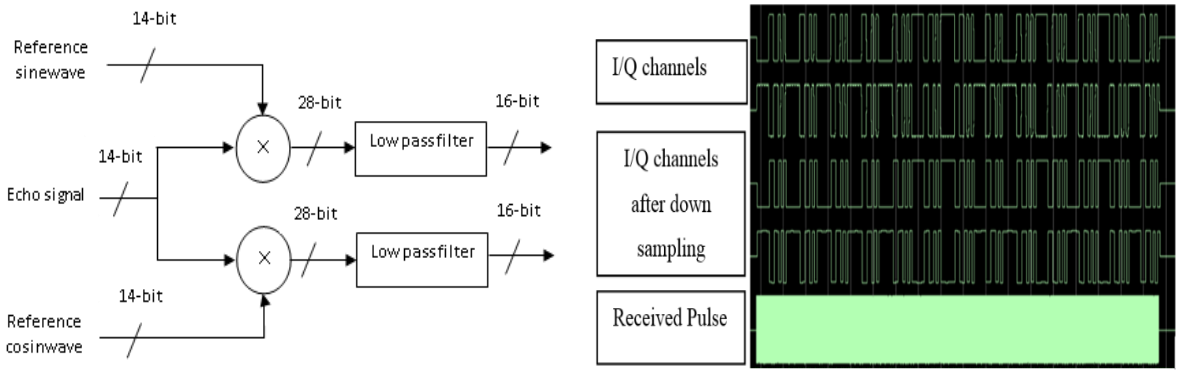


(a) (b)

Fig. (34) (a) Waveform generator block diagram, (b) The generated waveform on oscilloscope.

F.10 Digital Coherent Demodulator

The input to the receiver is a 30MHz waveform sampled using the ADS62P49/ADS4249 dual-channel 14-bit ADC at a sampling frequency of 245.76 MHz. A digital circuit is designed for demodulating the received signal based on the MATLAB calculations.The demodulator shown in Fig. (35a) consists of a digital multiplier which multiplies the input signal with reference Sine for the in-phase channel and reference Cosine for the quadrature-phase channels. Since the input word length is 14-bit, the output of the multiplier is 28-bit word length due to multiplication bit growth.The output of the multiplier is applied to the low pass filter for removing the high frequency components and leaving the envelope of the signal.The coefficients of the low pass filter are previously calculated using MATLAB, then the coefficient values are scaled to be used in the Filter IP core. The IP core input word length is 28-bit and the output word-length is 16-bit this is done using the truncation of least-significant bit option in the IP core as shown in Fig. (35b).

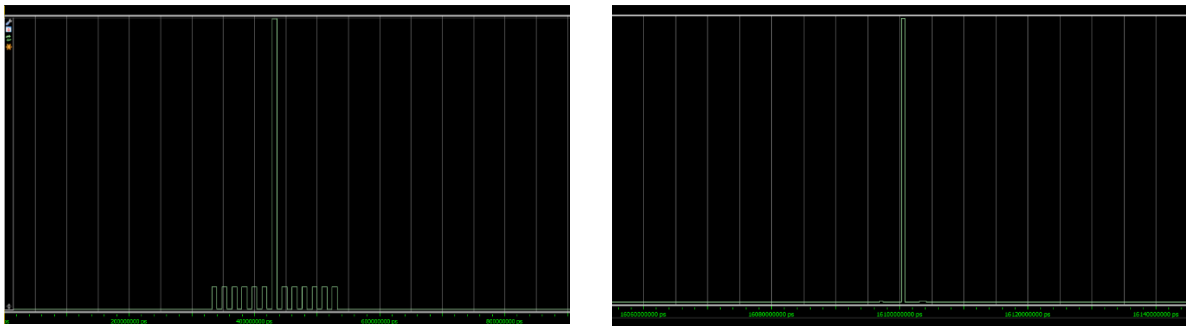


(a) (b)

Fig. (35): (a) Digital coherent-demodulator block diagram and (b) Its simulation results.

F.11 Matched Filter Implementation

The matched filter is implemented for both Barker-13 and compound Barker-169.In case of Barker-13, the matched filter is simply an FIR filter with 13 coefficients representing the replica of the Barker code. This can be done in different ways including VHDL design, schematic design, and Xilinx logicore IP FIR Compiler. For compound Barker 169, since the filter coefficients are the replica of the 169 Nested Barker code, it is not practical to implement it in time domain, and it is more convenient to be implemented using fast convolution (frequency domain filtering).The FFT of the replica for Barker 169 padded to the $T_r$length is calculated using MATLAB; then multiplied by the FFT of the optimum filter coefficients. The resulting real and imaginary values are stored in a ROM whose address is a counter that counts from zero to $T_r$and it resets every start of T_r.The input data from the coherent demodulator is applied to FFT, then the output of the FFT is multiplied with the output of the ROM, the product is then send to IFFT unit to convert it back to time domain. Single precision floating point is used during the matched filtering and optimum filtering processing to allow for high accuracy in calculations. However, Fig. (36a) and (36b) shows the matched filter output of Barker 13 and nested Barker 169, respectively.



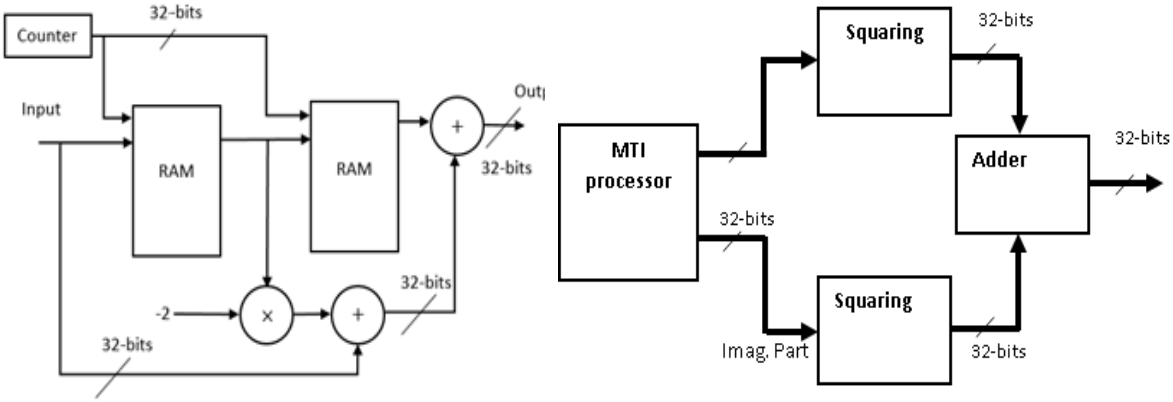
(a) (b)

Fig. (36) (a) Barker-13 simulation results and (b) Nested Barker 169 with side-lobe canceller simulation results.

F.12 MTI and Magnitude Calculator

The double delay canceller MTI, shown in Fig. (37-a) is designed using 2 block RAMs whose depth is equal to the number of range cells in each repetition period. The RAMs write enable is always set such that it stores the incoming data at each rising edge clock and output the old data of the previous period at the same edge, a counter is used to supply the RAMs with address. This counter is reset with the radar sync pulse.

The calculation of the magnitude is done without using square root in order to increase the SNR before CFAR processing. Both I and Q outputs of the MTI filters are applied to multipliers which works as a squaring circuit to calculate I^2 and Q^2. Both values are then sent to an adder, as shown in Fig. (37b).



(a) (b)

Fig. (37)(a) MTI and (b) Magnitude calculator block diagrams.

F.13 CFAR Implementation

The CFAR is implemented in single precession floating point, the addition is performed using recursive approach rather than non-recursive approach [30]. Fig. (38) shows the CFAR simulation results.

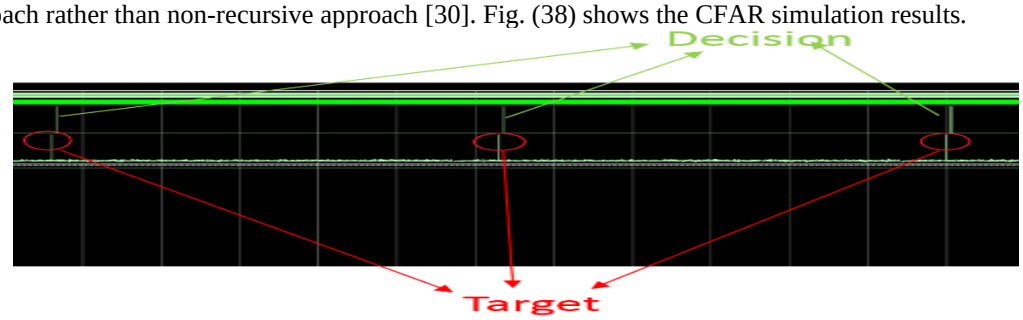


Fig. (38) CFAR real time results.

F.14 Total Device Utilization

The final design consists of the waveform generator, BIST unit and the signal processor.The design is implemented for both Barker 13 and Nested Barker 169 on the Xilinx Virtex-6 XC6VLX240T. Table 1 shows the device utilization for both Barker 13 and Nested Barker 169.The Nested Barker 169 processor consumes nearly twice the resources of the Barker 13 processor.

Table 1: The device utilization for both Barker 13 and Nested Barker 169

Required	Available	Barker 13	Nested Barker 169
Slice Registers	301,440	22,382(7%)	50,592(16%)
Slice LUTs	150,720	15,693(10%)	40,919(27%)
RAMB36E1/FIFO36E1s	416	26(6%)	53(12%)
RAMB18E1/FIFO18E1s	832	25(3%)	206(24%)
DSP48E1s	768	172(22%)	256(33%)

G. Control and Monitoring Subsystem

This system uses all the data from various subsystems and control the TURN-ON Sequence of a Radar Subsystem. It also keeps on monitoring and scanning all the critical parameters of subsystem and display the same with help of graphical user interface application on customer PC. The system block diagram is shown in Fig. (39). The proposed system is based on producing 4 bit address to isolation and fault isolation PCB's and receives the status throught 8 bit status bus. Another 8 bit are produced to control the operation of the system. Fig. (40) shows the functional diagram of the C/M system.

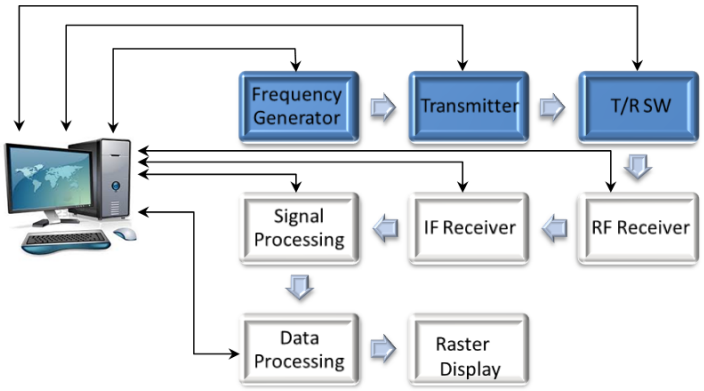


Fig. (39): C/M System Block diagram.

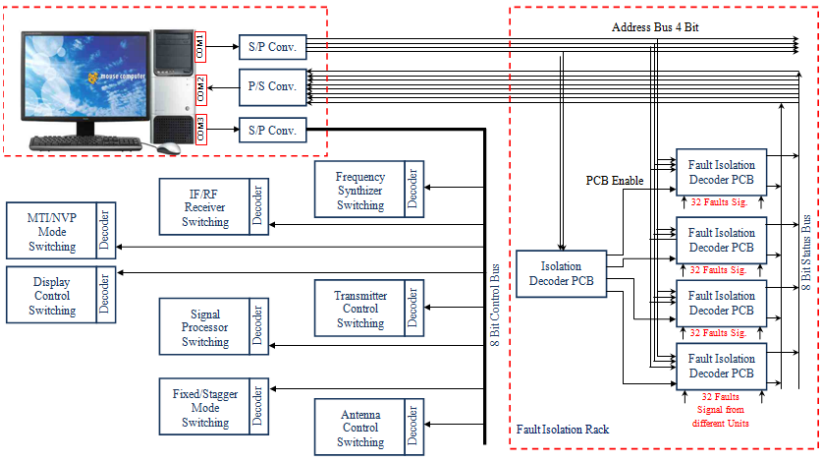


Fig. (40): Functional diagram of the C/M system.

Analog and digital signals in different radar sub-systems are monitored and tested by Control and Monitoring (C/M) system. Failures in radar systems may be classified to three categories based on their effect on performance: A which may damage some parts, B stops functionality, and C may degrade the system performance. For example, Power Amplifier (PA) modules may have one or more of these failure categories. Increasing the Voltage Standing Wave Ratio (VSWR) over specific value may damage the PA, which is considered class A. The PA biasing failure may stop its functionality, which will be considered class B failure. RF input level under certain threshold may degrade PA output level, thus it is considered class C. Class A (critical faults)requires high speed response to prevent damaging in the radar units. Mostly, preventing damaging action will be sent on control channels to different units immediately after problem detection. A Field Programmable Gate Array (FPGA) will be employed to take decisions and generate control signals in such situations because it handles high speed and parallel processing. Class B (stop functionality) may appear in biasing problems. Power supplies output may be applied to comparators to confirm the supply level. The error margin shall not affect the driven systems efficiency. In this case the decision to shut the system down or continue working is left to the user.

Class C (degrade efficiency) this type of failures doesn't need a live scanning, periodic scanning would be sufficient. RF input level under certain threshold is considered class C. The C/M just notify the user and the decision is left to him. Actions priority in CM are taken according to its class. Some of tests are just for monitoring to notify the operator to go out to maintenance or keep working. The signals to be tested has many forms. For digital buses, DACs are used to convert them to analog signals for displaying on oscilloscopes. These signals were multiplexed by the DSP. The data bus selection is done by the control and monitoring PC.RF signals are monitored using RF detectors to transform it to analog signals which can be applied to ADCs and then processed digitally using FPGA. Test points for example at the frequency generator are local oscillators output (IF/RF)and the modulated signal. These points are checked by the operator during daily, weekly, or monthly test procedures. While the power amplifier is very critical and sensitive system. So, supply (voltage and current), RF input (power level, duty cycle and pulse width), RF output (power level and VSWR) and temperature should be monitored accurately. To control and monitor PA we applied current sensors to monitor biasing current not to exceed the RF transistor maximum current. Temperature sensors were placed as close as possible to transistor junction and other thermal sensitive points. Thermal Threshold should be calculated considering max junction temperature, transistor case propagation, heat sink propagation, and a sufficient safe margin. Thermal fault counter actions were divided into two levels: cautions at slightly high temperature (class C), and forced transmitter shutdown at critical temperature (class A). The RF input amplitude check is done at each pulse, and controlled using an input switch to limit the input to the maximum PA pulse width and duty cycle. The output amplitude is measured to ensure the PA efficiency and check the VSWR. The VSWR is measured using two series directional couplers one for transmitted power while the other is for the reflections. A certain VSWR level shouldn't be exceeded so the user gets a caution at lower VSWR level (class C). For efficient control and monitoring all critical decisions is done automatically by the FPGA while cautions counter measures were left to the user.

H. Display and Data Processing System.

The display system is developed based on commercial of-the-shelf hardware and custom software. In order to view the received video from the DSP system, the plan position indicator (PPI) scope is used. PPI is used to present the air targets in polar coordinates that show the azimuth and range for targets and the screen center is the radar location. An air situation picture generated by using only radar video and antenna azimuth is called a raw video picture. Based on the raw video picture, two categories of data are visualized. The first is plots and tracks generated by automatic detection and tracking system. The second is display information that includes various maps, range marks, azimuth marks and any other information used by the operator.

H1. Display system components.

Display system contains the following components that are illustrated in Fig. (41). The components are categorized into hardware components and software (or modules) components. The hardware components include high performance industrial PC, industrial screen and data acquisition module. The data acquisition module is used to acquire the received plots from the DSP system via serial port RS232 controller and send the configuration commands back to DSP. The software components include two main blocks. First block is the operating system block that is Windows platform OS. However, the second block is display application that includes all software modules that work together to achieve the display function.

H2. Display software design.

To design suitable software architecture for air situation display, model-view-controller (MVC) and Observer design patterns are adopted. MVC pattern is used for developing user interface that is divided into three main parts.

- Model part that is the application structure independent of the user interface.
- View part represents the model data in graphical user interface (GUI) such as control panel or PPI screen.
- Controller part converts the user input into command for the model or view.

The Observer design pattern is used in event driven software systems. It defines one-to many dependencies between objects by defining one object that updates the state of dependent objects.

H3. Display application modules.

Each software module performs a function and contains local memory buffer that stores its data to be consumed by other modules. Software modules and their functions are described below.

Display preferences manager (DPM)- sets and stores the display preferences such as the map type, maximum range, radar location, screen intensity, etc. Data acquisition handler (DAH) - handles the received plots from the DSP unit and buffers them in a table that stores all plots associated data. Tracking – generate tracks from plots and store them in local buffer. Presentation manager (PM) - graphically displaying all elements of radar picture and handling user interaction. It includes: Plot renderer (PR) - render plots that are stored in DAH buffer on PPI screen according to their azimuth, range associated data. Track renderer (TR) - render tracks that are stored in the tracking local buffer and draw them on the PPI screen and show the required track information according to user configurations that is stored in DPM memory. Non-interactive graphic renderer (NIGR) - rendering fixed graphic object such as range and azimuth markers, code grid, maps and airways. In addition to, parsing geographic data files and determines coordinates. Interactive graphic manager (IGM) - rendering and handling user interaction with tracks and graphics objects.

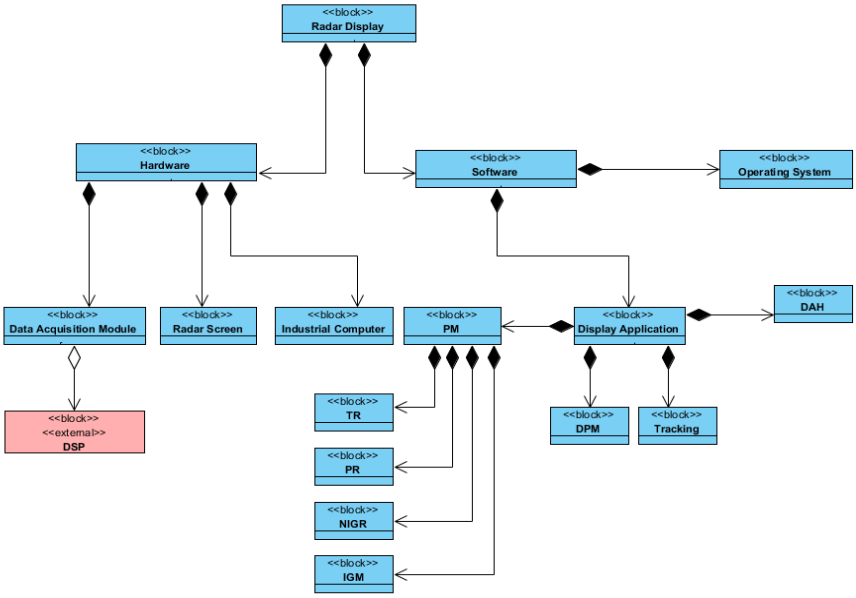


Fig. (41): Display system clock diagram.

H4. Implementation:

Display implantation is developed. Net framework is written in C# programming language that is very common language for different types of windows applications. PPI Implementation is done in layers architecture. Each layer represents the output software module and all layers are added to generate the final view for the PPI display. Fig. (42) illustrates the result of adding all display layer in a final layer.

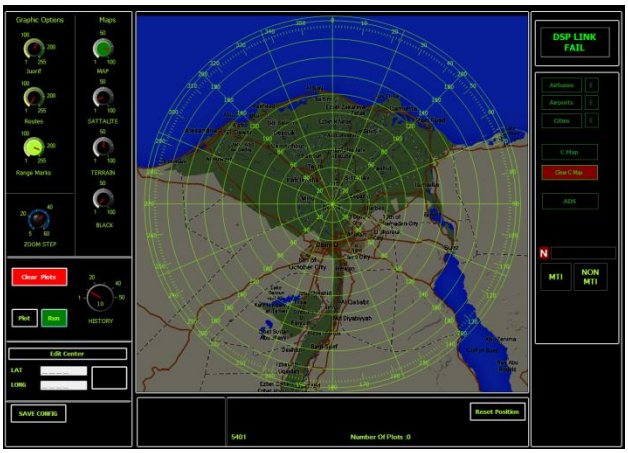


Fig. (42): Final display result.

III. Conclusion

The main purpose of this paper is to demonstrate the design, implementation and industrial system engineering perspectives for the Egyptian radar ESR-32A which had been presented in EDEX-2018 exhibition. The radar is reliable L-band surveillance radar designed as an unattended system intended to operate while simultaneously performing system self tests, reporting status and surveillance data to the Air Traffic Control System. Apart from the antenna, transmitter and waveguide components, the equipment in the system is configured in dual channels to provide a totally redundant system. Cross connections between redundant modules permit additional failures to occur while the system continues in operation, in comparison to other systems. The transmitter is implemented using 25 % redundancy providing inherent high reliability with a fail-

soft operation. The configuration of the radar consists of a terminal approach radar to 150 Km with a rotation rate of 5 rpm.

REFERENCES

[1] Jeffrey R. Homola, Lynne H. Martin, Joey S. Mercer and Christopher C. Cabrall,"Automated Air Traffic Control Operations with Weather and Time-Constraints," Ninth USA/Europe Air Traffic Management Research and Development Seminar (ATM2011).

[2] Blanchard,"Systems Engineering Management", Third Edition. John Wiley & Sons, 2004.

[3] H. Eisner,"Essentials of Project and Systems Engineering Management," Second Edition. John Wiley & Sons, 2002.

[4] D. Buede ,"The Engineering Design of Systems: Models and Methods", Second Edition, John Wiley & Sons, 2009.

[5] Department of Defense, "Systems Engineering Guide for Systems of Systems", DUSD (A & T) and OSD (AT & L), 2008.

[6] M. Jamshidi," System of Systems Engineering: Innovations for the 21st Century", John Wiley & Sons, 2008.

[7] M. Jamshidi," Systems of Systems Engineering: Principles and Applications", CRC Press, 2008.

[8] M. Maier and E. Rechtin ,"The Art of Systems Architecting", CRC Press , 2009, 3rd edition.

[9] A. Sage and S. Biemer, "Processes for system family architecting, design and integration", IEEE Systems Journal, 2007.

[10] A. Sage and C. Cuppan,"On the systems engineering and management of systems and federations of systems, "Information Knowledge Systems Management, 2001, 2 (4), 325 – 345.

[11] A. D. Hall,"A Methodology for Systems Engineering", Van Nostrand , 1962 , Chapter 4.

[12] N. B. Reilly,"Successful Systems for Engineers and Managers," Van Nostrand Reinhold, 1993.

[13] Philippe Lacomme, Jean-Philippe Hardange,Jean-Claude Marchais, Eric Normant " Air and Spaceborne Radar Systems." 2001.

[14] Richard J. Wiegand " Radar electronic countermeasures system design." Artech House, 1991.

[15] Richard curry " Radar system performance modeling." Artech House, 2005.

[16] Simon Kingsley ,Shaun quean" Understanding radar system." Scitech Publishing, 1992.

[17] Harry L. Van Trees " Detection, Estimation, and Modulation Theory." John Wiley, 2001.

[18] Nadav Levanon, Mozeson " Radar signals." John Wiley, 2004.

[19] J. Laskar, B. Matinpour, and S. Chakraborty,"Modern Receiver Front-Ends," John Wiley & Sons, Inc, USA, 2004.

[20] L. W. Couch,"Digital and Analog Communication Systems," Macmillan, New York, 1993.

[21] Merrill I. Skolnik, "Radar Handbook", McGraw-Hill, New York, 2007.

[22] Nadav Levanon" Non coherent pulse compression." IEEE Transaction on Aerospace and Electronic Systems, vol .42, No.2, pp. 756-765, April 2006.

[23] Bassem R. Mahafza " Radar systems analysis and design using MATLAB." Chapman & Hall/CRC 2004.

[24] Chengchang Zhang and Lihong Zhang, "Intermediate Frequency Digital Receiver Based on Multi-FPGA System", Journal of Electrical and Computer Engineering, vol. 2016, Article ID 6123832, 8 pages, 2016.

[25] Merril I. Skolnik, Introduction to radar systems (3rd ed.), McGraw-Hill, (2001).

[26] E. C. lfeacher, Digital Signal Processin, A Practical Approach, Prentice Hall, 2002.

[27] B. A. S. A. Abd El-Rahman H. Elbardawiny , C. Fathy M. Ahmed and D. Mamdouh Hassan, "A Novel Sidelobe Cancellation Method for Binary Barker Code Pulse Compression," 17th International Conference On Aerospace Sciences & Aviation Technology, April 11 - 13 2017.

[28] B. R. Mahafza, Matlab Simulations for Radar Systems Design, Chapman & Hall/CRC, 2004.

[29] A. M. A. Razik and F. M. Ahmed, "FPGA Based Waveform Generator and BIST unit for Binary Phase Coded Pulse Compression Radar", Journal of Multidisciplinary Engineering Science and Technology (JMEST), Vol. 4, Issue 1, PP.6504-6507, January - 2017

[30] F. M. A. Kader, Nabil G. Mechael, and Ali M. Abou Zeid, "Analysis and design of a modified GO-CFAR processor – Hardware implementation using PLDs," in Proceeding of the 2nd ICEENG Conference, M.T.C, Cairo, Egypt 1999.

Technical Crew

Degree	Name	Affiliation
Prof. Dr.	Ashraf Shawky Selium	Microstrip Dept., Electronics Research Institute
Prof. Dr.	Ahmed Mohamed Attia	Microwave Dept., Electronics Research Institute
Ass. Prof. Dr.	Haytham Hussein Abdulla	Microwave Dept., Electronics Research Institute
Ass. Prof. Dr.	Dalia Mohamed Nashaat	Microstrip Dept., Electronics Research Institute
Ass. Prof. Dr.	Tamer Gaber Mohamed Ali	Microstrip Dept., Electronics Research Institute
Dr.	Hesham Abd-El-Hady Mohamed	Microstrip Dept., Electronics Research Institute
Dr.	Mohamed Shaker Abd-El-Fattah	Microstrip Dept., Electronics Research Institute
Eng.	Osama Mohamed Dardeer	Microstrip Dept., Electronics Research Institute
Eng.	Hesham Yamani	Microwave Dept., Electronics Research Institute
Eng.	Amgad Ahmed Said	Faculty of Engineering, Ain Shams University
Dr.	Mohamed Shalaby	Faculty of Engineering, Arab Academy of Science, Technology and Maritime
Dr.	Walid M. Saad	Faculty of Engineering, Alexandria University
Dr.	Abdelrahman M. El-Akhdar	Faculty of Engineering, Ain Shams University
Dr.	Ahmed Alieldin	Faculty of Engineering, The university of Alexandria
Eng.	Mahmoud F. Abd Elzaher	Faculty of Engineering, Ain Shams University
Eng.	Ahmed E. Mansour	Faculty of Engineering, Ain Shams University
Eng.	Ahmed S. I. Amar	Faculty of Engineering, Ain Shams University
Eng.	Bahaaeldin M. F. Elsor	Faculty of Engineering, Alexandria University
Eng.	Hossam M. Hassan	Faculty of Engineering, Alexandria University
Eng.	Kamal Hussein Mustafa	Faculty of Engineering, Ain Shams University
Eng.	Mostafa Hamed Abdalla	Faculty of Engineering, Cairo University
Eng.	Alla M. Eid	Faculty of Engineering, Alexandria University
Eng.	Mohammad M. Abdul-Atty	Faculty of Engineering, Ain Shams University
Eng.	Anas E. Elfaramawy	Faculty of Engineering, Ain Shams University
Eng.	Ahmed Hosny Shora	Faculty of Engineering, Al Azhar University
Eng.	Ahmed F. El-Agamy	Faculty of Engineering, Alexandria University
Eng.	Moustafa Yassen Mohamed	Faculty of Engineering, Alexandria University